Radio Shack®

Service Manual

26-3612

TRS-80®

Pocket Computer RS-232C Interface

Catalog Number: 26-3612

CUSTOM MANUFACTURED FOR RADIO SHACK, A DIVISION OF TANDY CORPORATION

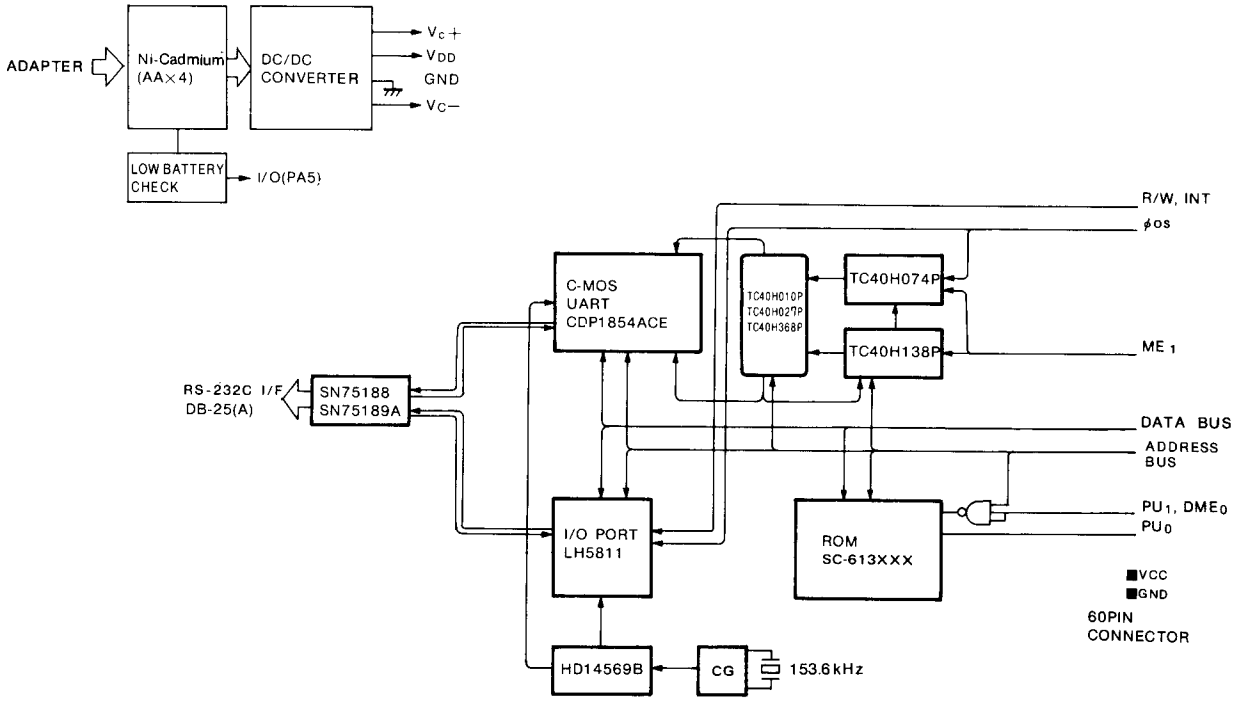
CONTENTS

SPECIFICATIONS

Transmission Method	:	Asynchronous
Applicable Standards	:	EIA RS-232C compliance
Baud Rate	:	50, 100, 110, 200, 300, 600, 1200, 2400 baud, programmable*
Data Bit	:	5, 6, 7, 8 bits, programmable
Parity Bit	:	Even, odd, non-parity, programmable
Stop Bit	:	1 or 1.5 for the character size of 5. 1 or 2 for the character sizes of 6 to 8. } programmable
Connectors Used	:	60-pin male connector for the PC-2 or Printer/Cassette Interface. 25-pin connector, DB-25(W), for an external device. Power Adapter jack.
Power Supply Source	:	4.8 V ⎓ (DC): Ni-Cadmium rechargeable battery AC: 120 V, 60 Hz with Adapter
Power Consumption	:	4.8 V ⎓ (DC), 0.80 W
Battery Capacity	:	For approx. 3 hours of operation (charging: 15 hours)
Output Signal Level	:	High level: +5 V to +10 V (3 to 7 kohms load) Low level: −5 V to −10 V (3 to 7 kohms load)
Interfacing Signals	:	Inputs: RD, DSR, CD, CTS Outputs: TD, RTS, DTR Others: SG (FG)
Switch	:	POWER switch
Dimensions	:	86 mm (W) x 115 mm (D) x 50 mm (H) 3-3/8″ (W) x 4-17/32″ (D) x 1-31/32″ (H)
Weight	:	435 g (0.96 lbs)
Accessories	:	Keyboard templates, joint plates (two kinds) and instruction manual.

* : In terminal program mode, the specifications of baud rate (600, 1200 and 2400) are restricted.

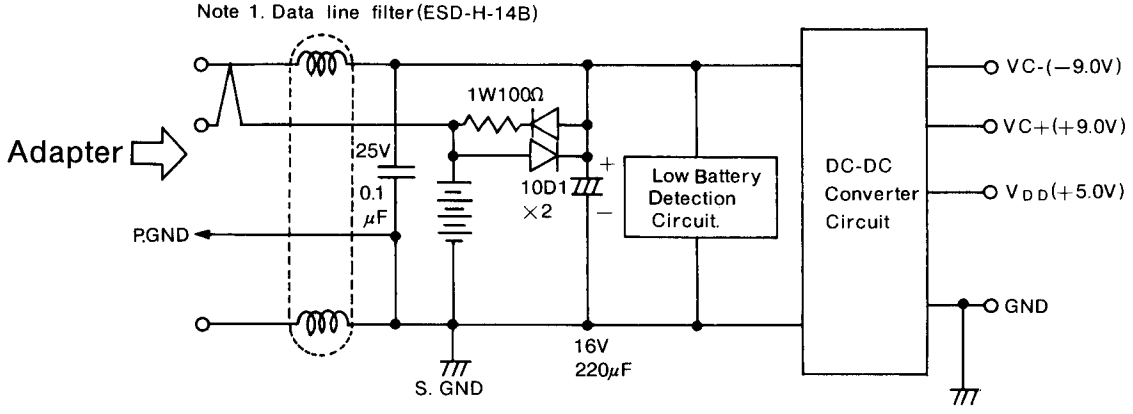
BLOCK DIAGRAM



CIRCUIT DESCRIPTION

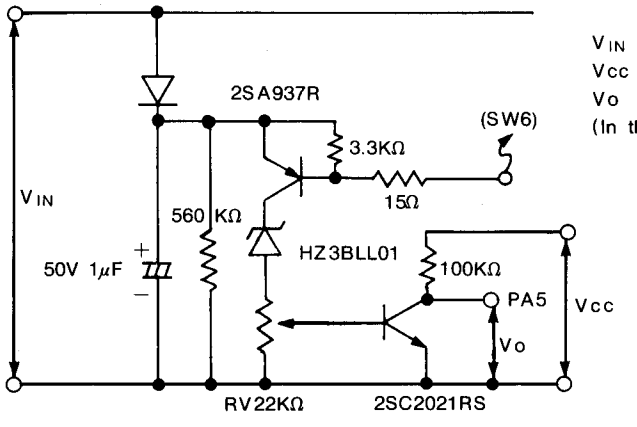
- **Power supply**

The Interface is driven by the PC-2 power (Vcc) and Ni-Cadmium battery, or through an AC adapter.
The input is fed through the DC-DC converter to get VDD (+5.0 V), VC+ (+9.0 V), and VC- (-9.0 V).

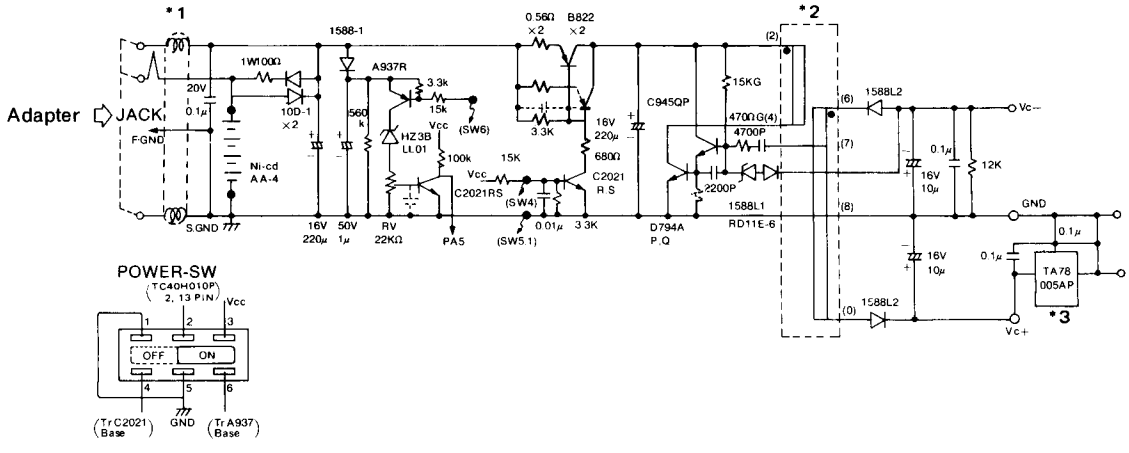


- **Low battery detection circuit**

Battery condition is monitored by the circuit shown below. Signals detected are checked by the CPU for each receiving and transmitting step through LH5811's PA5 I/O port. When, SW6 reaches the GND level with power on, 2SA937R is turned on to keep the low battery detection circuit functioning.



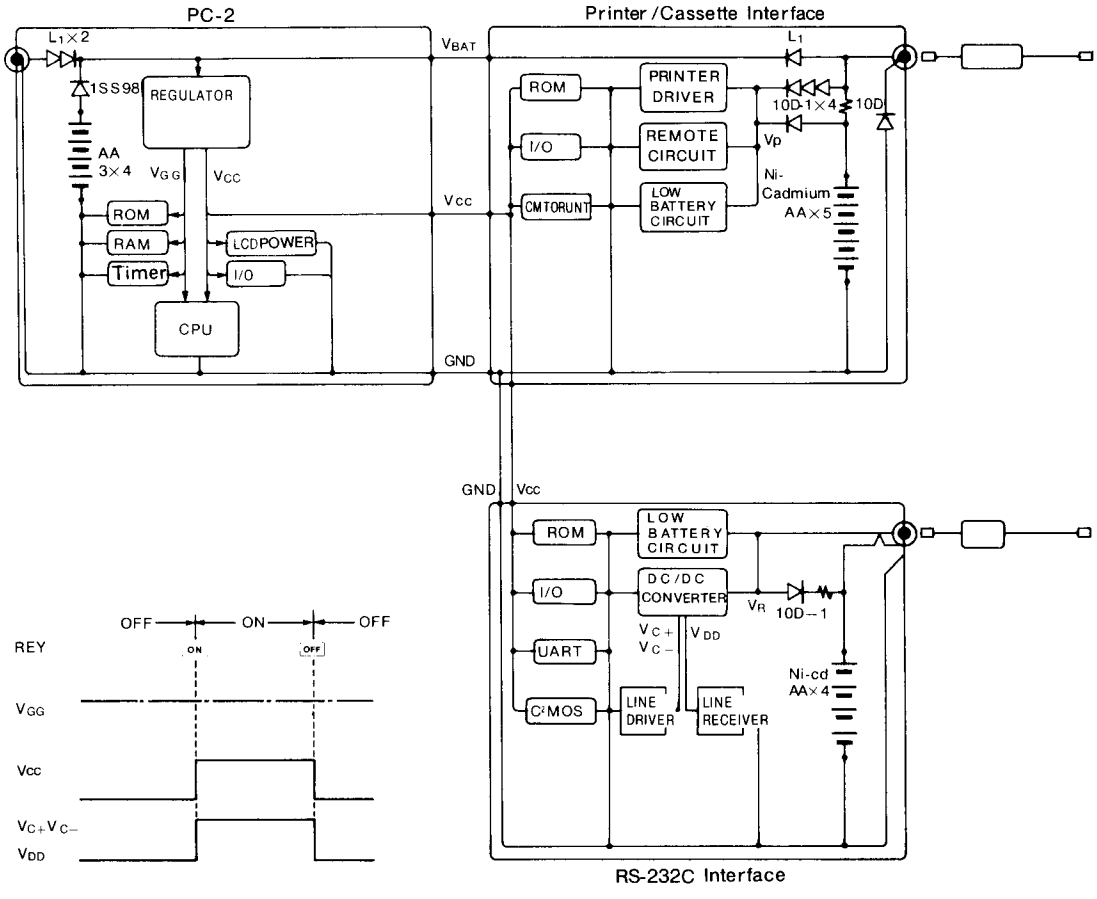
V_{IN} : 4.40V±0.01V
Vcc : 4.0V±0.1V
Vo : 1.0V±0.1V
(In the case of 25°C±1°C)

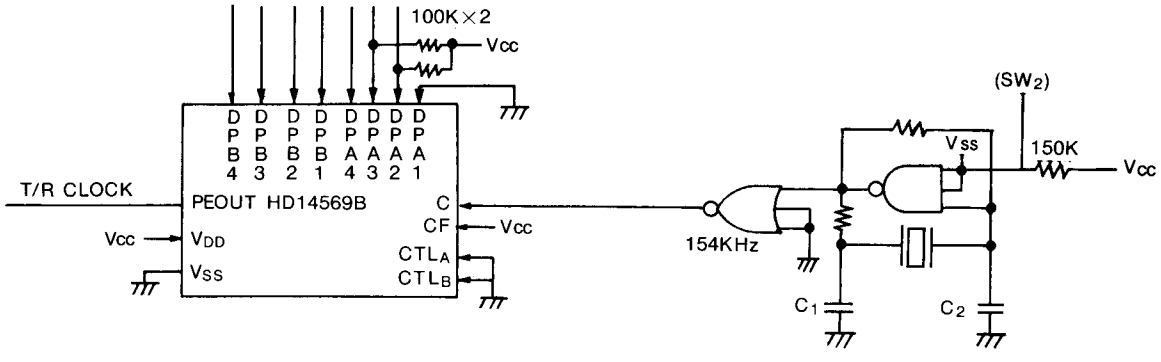


Note: While the power switch is on, SW4 and SW5 remain open to each other. Vcc is pressed to the base of 2SC2021, and 2SC2021 and 2SB822 are turned on.

*1) Data line filter (ESD-H-14B)
*2) Converter H1750
*3) 3-terminal regulator

POWER SOURCE (PC-2, Printer/Cassette Interface, RS-232C Interface)





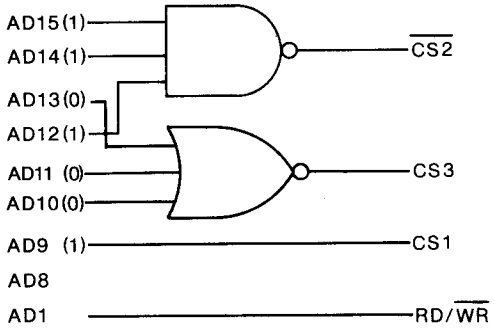
- **CLOCK circuit**

  According to commands from the CPU, the frequency dividing ratio is changed to make a clock pulse correspond to selected baud rates. In the initial setting, after turning the power switch on, a baud rate of 300 is automatically provided. A specified baud rate can be obtained with a change command from the CPU. The commands are delivered to LH5811 ports PC0 through PC4, PA6 or PA7. (T/R clock = baud rate X 16)

- **CDP1854ACE CHIP SELECT**

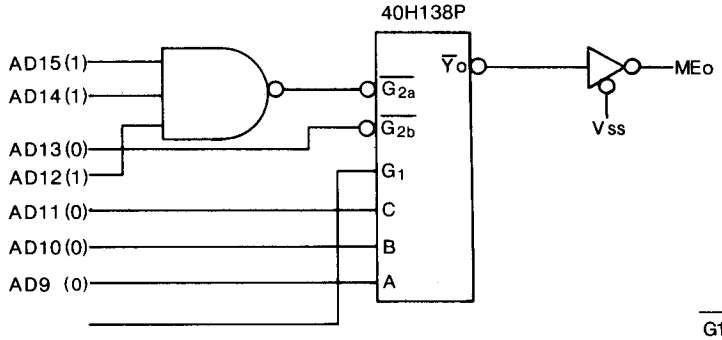
  To select this chip, CS1 and CS3 must be HIGH and $\overline{CS2}$ must be LOW.

  The circuit is as shown below.



(Address D200 ..... WRITE
  D201 ..... READ)

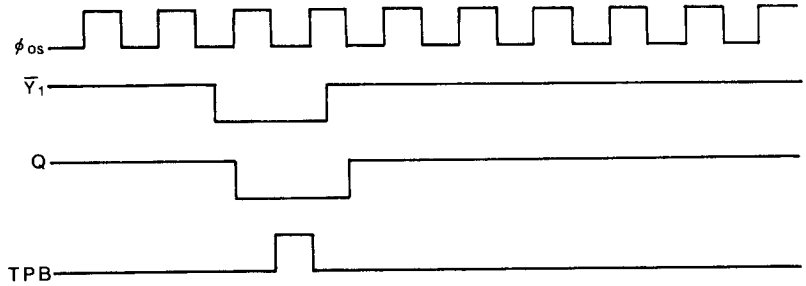
- **LH5811 CHIP SELECT**

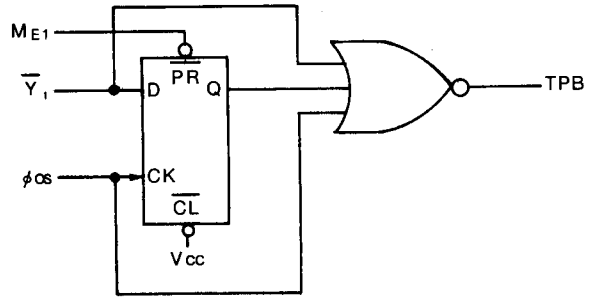


(Address D000 or D00F to be used).

$\overline{G1 \cdot \overline{G2a} \cdot \overline{G2b} \cdot \overline{A} \cdot \overline{B} \cdot \overline{C}} = M_{EO}$

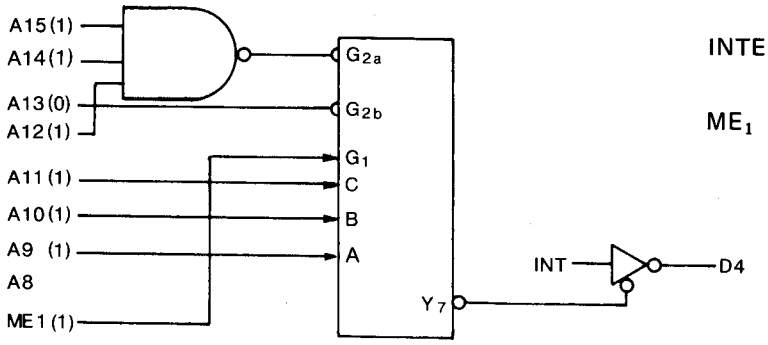
- **TPB CIRCUIT**





The left-hand circuit produces one pulse at ME_1 ($\overline{Y_1}$). At Y_1 and ϕOS, however, two pulses are generated up to TPB. Therefore, a stage of DFF is added to produce signal O. Thus TPB consists of Y_1, Q, and ϕOS.

- **INT CIRCUIT**



INTERRUPT PORT ADDRESS

ME_1 (DE00 ~ DFFF)

LSI DESCRIPTION

LH5811

LH5811 is C-MOS I/O port and detail of this LSI is explained in the Service Manual 26-3601/3605. Therefore, please refer it.

CDP1854A, CDP1854AC Types

1. Initialization and Controls

In this mode, the CDP1854A is configured to receive commands and send status via the microprocessor data bus. The register connected to the transmitter bus or the receiver bus is determined by the RD/WR and RSEL inputs as follows:

Table 1. Register Selection Summary

RSEL	RD/WR	Function
Low	Low	Load Transmitter Holding Register from Transmitter Bus
Low	High	Read Receiver Holding Register from Receiver Bus
High	Low	Load Control Register from Transmitter Bus
High	Low	Read Status Register from Receiver Bus

In this mode, the CDP1854A is compatible with a bidirectional bus system. The receiver and transmitter buses are connected to the bus. The CLEAR input is pulsed, resetting the Control, Status, and Receiver Holding Registers and setting SERIAL DATA OUT (SDO) high. The Control Register is loaded from the Transmitter Bus to determine the operating configuration for the UART. Data is transferred from the Transmitter Bus inputs to the Control Register during TPB when the UART is selected (CS1 · CS2 · CS3-1) and the Control Register is designated (RSEL = H. RD/$\overline{WR}$ = L). The CDP1854A also has a Status Register which can be read onto the Receiver Bus (R BUS 0-R BUS 7) to determine the status of the UART.

2. Transmitter Operation

Before beginning to transmit, the TRANSMIT REQUEST (TR) bit in the Control Register (see bit assignment, Figure 3) is set. Loading the Control Register with TR = 1 (bit 7 = high) inhibits changing the other control bits. Therefore, two loads are required–one to format the UART, the second to set TR. When TR has been set, a TRANSMITTER HOLDING REGISTER EMPTY ($\overline{THRE}$) interrupt will occur, signalling the microprocessor that the Transmitter Holding Register is empty and may be loaded. Setting TR also causes assertion of a low level on the REQUEST TO SEND (RTS) output to the peripheral. It is not necessary to set TR for proper operation of the UART. If desired, it can be used to enable $\overline{THRE}$ interrupts and to generate the $\overline{RTS}$ signal. The Transmitter Holding Register is loaded from the bus by TPB during execution of an output instruction. The CDP1854A is selected by CS1 · CS2 · CS3 = 1, and the Holding Register is selected by RSEL = L and RD/$\overline{WR}$ = L. When the $\overline{CLEAR\ TO\ SEND}$ ($\overline{CTS}$) input (which can be connected to a peripheral device output) goes low, the Transmitter Shift Register will be loaded from the Transmitter Holding Register and data transmission will begin. If CTS is always low, the Transmitter Shift Register will be loaded on the first high-to-low edge of the clock which occurs at least 1/2 clock period after the trailing edge of TPB; transmission of a start bit will occur 1/2 clock period later (see Figure 1). Parity (if programmed) and stop bit(s) will be transmitted following the last data bit. If the word length selected is less than 8 bits, the most significant unused bits in the Transmitter Shift Register will not be transmitted.

On the transmitter clock period after the Transmitter Shift Register is loaded from the Transmitter Holding Register, the $\overline{THRE}$ signal will go low and an interrupt will occur ($\overline{INT}$ goes low). The next character to be transmitted can then be loaded into the Transmitter Holding Register for transmission with its start bit immediately following the last stop bit of the previous character. This cycle can be repeated until the last character is transmitted, at which time a final THRE · TSRE interrupt will occur. This interrupt signals the microprocessor that TR can be turned off. This is done by reloading the original control byte in the Control Register with the TR bit = 0, thus terminating the $\overline{REQUEST\ TO\ SEND}$ ($\overline{RTS}$) signal.

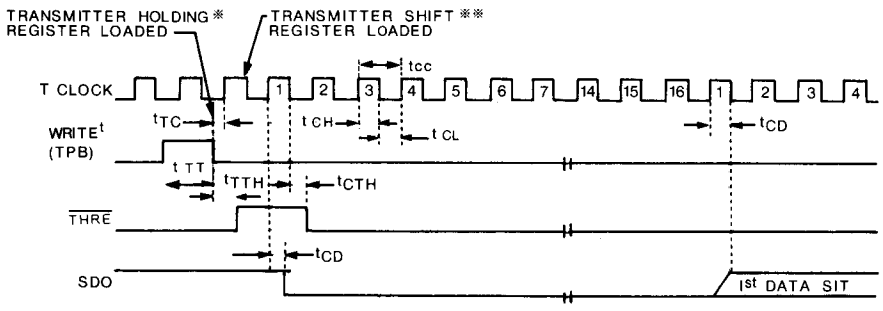
SERIAL DATA OUT (SDO) can be held low by setting the BREAK bit in the Control Register (see Figure 3). SDO is held low until the BREAK bit is reset.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85°C, V_{DD} ±5 %, t_r, t_f − 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, C_L = 100 pF. See Figures 1 and 2.

CHARACTERISTIC		V_{DD} (V)	LIMITS				UNITS
			CDP1854A		CDP-1854A		
			Typ. •	Max. ▲	Typ. •	Max. ▲	
Transmitter Timing – MODE 1							
Minimum Clock Period	t_{CC}	5 10	250 125	310 155	250 –	310 –	ns
Minimum Pulse Width: Clock Low Level	t_{CL}	5 10	100 75	125 100	100 –	125 –	ns
Clock High Level	t_{CH}	5 10	100 75	125 100	100 –	125 –	ns
TPB	t_{TT}	5 10	100 50	150 75	100 –	150 –	ns
Minimum Setup Time: TPB to Clock	t_{TC}	5 10	175 90	225 150	175 –	225 –	ns
Propagation Delay Time: Clock to Data Start Bit	t_{CD}	5 10	300 150	450 225	300 –	450 –	ns
TPB to $\overline{THRE}$	t_{TTH}	5 10	200 100	300 150	200 –	300 –	ns
Clock to $\overline{THRE}$	t_{CTH}	5 10	200 100	300 150	200 –	300 –	ns
CPU Interface – WRITE Timing – MODE 1							
Minimum Pulse Width: TPB	t_{TT}	5 10	100 50	150 75	100 –	150 –	ns
Minimum Setup Time: RSEL to Write	t_{RSW}	5 10	50 25	74 40	50 –	75 –	ns
Data to Write	t_{DW}	5 10	−100 −50	−75 −35	100 –	−75 –	ns
Minimum Hold Time: RSEL after Write	t_{WRS}	5 10	50 25	75 40	50 –	75 –	ns
Data after Write	t_{WD}	5 10	75 40	125 60	75 –	125 –	ns

• Typical values are for T_A = 25°C and nominal voltages.

▲ Maximum limits of minimum characteristics are the values above which all devices function.

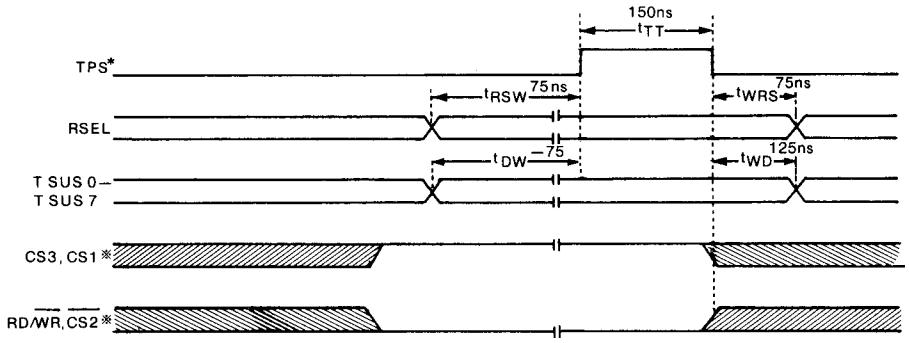


* THE HOLDING REGISTER IS LOADED ON THE TRAILING EDGE OF TPB.

** THE TRANSMITTER SHIFT REGISTER IS LOADED ON THE FIRST HIGH-TO-LOW TRANSITION OF THE CLOCK WHICH OCCURS AT LEAST 1/2 CLOCK PERIOD $+t_{TC}$ AFTER THE TRAILING EDGE OF TPB, AND TRANSMISSION OF A START BIT OCCURS 1/2 CLOCK PERIOD + t_{CD} LATER.

t WRITE IS THE OVERLAP OF TPB, CS1, AND CS3 = 1 AND $\overline{CS2}$, RD/$\overline{WR}$ = O.

Figure 1. Transmitter Timing Diagram – MODE 1 .



* WRITE IS THE OVERLAP OF TPB, CS1, CS3 = 1 AND $\overline{CS2}$, RD/$\overline{WR}$ = O.

Figure 2. MODE 1 CPU Interface (WRITE) Timing Diagram.

CONTROL REGISTER BIT ASSIGNMENT TABLE

Bit	7	6	5	4	3	2	1	0
Signal	TR	BREAK	IE	WLS2	WLS1	SBS	EPE	PI

Bit Signal: Function

0 PARITY INHIBIT (PI):
When set high, parity generation and verification are inhibited and the PE Status bit is held low. If parity is inhibited, the stop bit(s) will immediately follow the last data bit on transmission, and EPE is ignored.

1 EVEN PARITY ENABLE (EPE):
When set high, even parity is generated by the transmitter and checked by the receiver. When low, odd parity is selected.

2 STOP BIT SELECT (SBS):
See table below.

3 WORD LENGTH SELECT 1 (WLS1):
See table below.

4 WORD LENGTH SELECT 2 (WLS2):
See table below.

Bit 4 WLS2	Bit 3 WLS1	Bit 2 SBS	Function
0	0	0	5 data bits, 1 stop bit
0	0	1	5 data bits, 1.5 stop bits
0	1	0	6 data bits, 1 stop bit
0	1	1	6 data bits, 2 stop bits
1	0	0	7 data bits, 1 stop bit
1	0	1	7 data bits, 2 stop bits
1	1	0	8 data bits, 1 stop bit
1	1	1	8 data bits, 2 stop bits

Figure 3. Control Register Bit Assignment.

5 INTERRUPT ENABLE (IE):
When set high, $\overline{\text{THRE}}$, DA, THRE · TSRE, $\overline{\text{CTS}}$, and PSI interrupts are enabled (see Interrupt Conditions, Table II).

6 TRANSMIT BREAK (BREAK):
Holds SDO low when set. Once the break bit in the control register has been set high, SDO will stay low until the break bit is reset low and one of the following occurs: $\overline{\text{CLEAR}}$ goes low; $\overline{\text{CTS}}$ goes high; or a word is transmitted. (The transmitted word will not be valid since there can be no start bit if SDO is already low. SDO can be set high without intermediate transitions by transmitting a word consisting of all zeros.)

7 TRANSMIT REQUEST (TR):
When set high, $\overline{\text{RTS}}$ is set low and data transfer through the transmitter is initiated by the initial $\overline{\text{THRE}}$ interrupt. (When loading the Control Register from the bus, this (TR) bit inhibits changing of other control flip-flops.)

3. Receiver Operation

The receive operation begins when a start bit is detected at the SERIAL DATA IN (SDI) input. After detection of the first high-to-low transition on the SDI line, a valid start bit is verified by checking for a low-level input 7-1/2 receiver clock periods later. When a valid start bit has been verified, the following data bits, parity bit (if programmed) and stop bit(s) are shifted into the Receiver Shift Register by clock pulse 7-1/2 in each bit time. The parity bit (if programmed) is checked and receipt of a valid stop bit is verified. On count 7-1/2 of the first stop bit, the received data is loaded into the Receiver Holding Register. If the word length is less than 8 bits, zeros (low output level) are loaded into the unused most significant bits. If $\overline{\text{DATA AVAILABLE}}$ ($\overline{\text{DA}}$) has not been reset by the time the Receiver Holding Register is loaded, the OVERRUN ERROR (OE) status bit is set. One half clock period later, the PARITY ERROR (PE) and FRAMING ERROR (FE) status bits become valid for the character in the Receiver Holding Register. At this time, the Data Available status bit is also set and the $\overline{\text{DATA AVAILABLE}}$ ($\overline{\text{DA}}$) and $\overline{\text{INTERRUPT}}$ ($\overline{\text{INT}}$) outputs go low, signalling the microprocessor that a received character is ready. The microprocessor responds by executing an input instruction. The UART's 3-state bus drivers are enabled when the UART is selected (CS1 · CS2 · CS3 = 1) and RD/$\overline{\text{WR}}$ = high. Status can be read when RSEL = high. Data is read when RSEL = Low. When reading data, TPB latches data in the microprocessor and resets $\overline{\text{DATA AVAILABLE}}$ ($\overline{\text{DA}}$) in the UART. The preceding sequence is repeated for each serial character which is received from the peripheral.

STATUS REGISTER BIT ASSIGNMENT TABLE

Bit	7	6	5	4	3	2	1	0
Signal	THRE	TSRE	PSI	ES	FE	PE	OE	DA
Also Available at Terminal	22*	–	–	–	14	15	15	19*

* Polarity reversed at output terminal.

Figure 4. Status Register Bit Assignment

BIT SIGNAL: FUNCTION

0 DATA AVAILABLE (DA):
When set high, this bit indicates that an entire character has been received and transferred to the Receiver Holding Register. This signal is also available at Term. 19, but with its polarity reversed.

1 OVERRUN ERROR (OE):
When set high, this bit indicates that the Data Available bit was not reset before the next character was transferred to the Receiver Holding Register. This signal is OR'ed when PE is output at Term. 15.

2 PARITY ERROR (PE):
When set high, this bit indicates that the received parity bit does not match the bit programmed by the EVEN PARITY ENABLE (EPE) control. This bit is updated each time a character is transferred to the Receiver Holding Register. This signal is OR'ed when OE is output at Term. 15.

3 FRAMING ERROR (FE):
When set high, this bit indicates that the received character has no valid stop bit, i.e., the bit following the parity bit (if programmed) is not a high-level voltage. This bit is updated each time a character is transferred to the Receiver Holding Register. This signal is also available at Term. 14.

4 EXTERNAL STATUS (ES):
This bit is set high by a low-level input at Term. 38 ($\overline{\text{ES}}$).

5 PERIPHERAL STATUS INTERRUPT (PSI):
This bit is set high by a high-to-low voltage transition of Term. 37 ($\overline{\text{PSI}}$). The INTERRUPT output (Term. 13) is also asserted ($\overline{\text{INT}}$ = Low) when this bit is set.

6 TRANSMITTER SHIFT REGISTER EMPTY (TSRE):

When set high, this bit indicates that the Transmitter Shift Register has completed serial transmission of a full character, including stop bit(s). It remains set until the start of transmission of the next character.

7 TRANSMITTER HOLDING REGISTER EMPTY (THRE):

When set high, this bit indicates that the Transmitter Holding Register has transferred its contents to the Transmitter Shift Register and may be reloaded with a new character. Setting this bit also sets the $\overline{THRE}$ output (Term. 22) low and causes an INTERRUPT ($\overline{INT}$ = low), if TR is high.

4. Peripheral Interface

In addition to serial data in and out, four signals are provided for communication with a peripheral. The $\overline{REQUEST\ TO\ SEND}$ ($\overline{RTS}$) output signal alerts the peripheral to get ready to receive data. The $\overline{CLEAR\ TO\ SEND}$ ($\overline{CTS}$) input signal is the response, signalling that the peripheral is ready. The $\overline{EXTERNAL\ STATUS}$ ($\overline{ES}$) input latches a peripheral status level, and the $\overline{PERIPHERAL\ STATUS\ INTERRUPT}$ ($\overline{PSI}$) input senses a status edge (high-to-low) and also generates an interrupt. For example, the modern $\overline{DATA\ CARRIER\ DETECT}$ line could be connected to the $\overline{PSI}$ input on the UART in order to signal the microprocessor that transmission failed because of loss of the carrier on the communications line. The PSI and ES bits are stored in the Status Register (see Figure 4).

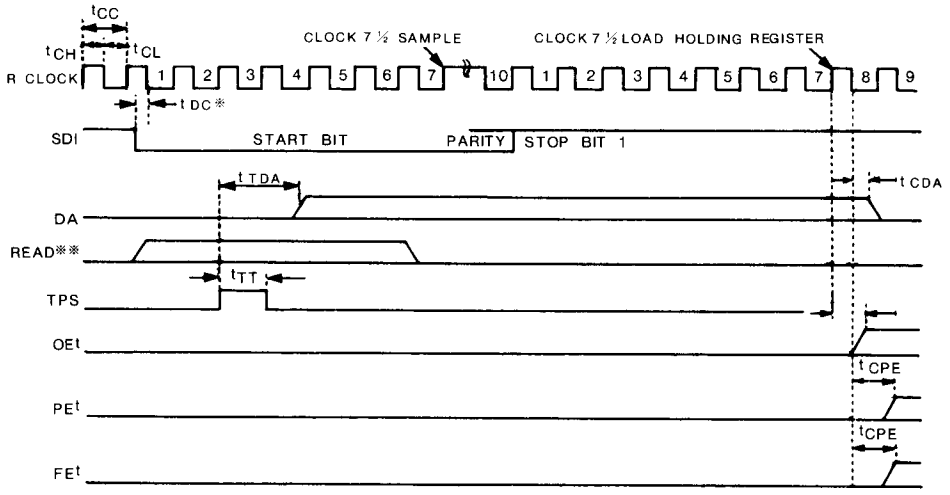


Figure 5. MODE 1 Receiver Timing Diagram.

* IF A START BIT OCCURS AT A TIME LESS THAN t_{DC} BEFORE A HIGH-TO-LOW TRANSITION OF THE CLOCK, THE START BIT MAY NOT BE RECOGNIZED UNTIL THE NEXT HIGH-TO-LOW TRANSITION OF THE CLOCK; THE START BIT MAY BE COMPLETELY ASYNCHRONOUS WITH THE CLOCK.

** READ IS THE OVERLAP OF CS1, CS3, RD/$\overline{WR}$ = 1 AND $\overline{CS2}$ = 0.
IF A PENDING DA HAS NOT BEEN CLEARED BY A READ OF THE RECEIVER HOLDING REGISTER BY THE TIME A NEW WORD IS LOADED INTO THE RECEIVER HOLDING REGISTER, THE OE SIGNAL WILL BE HIGH.

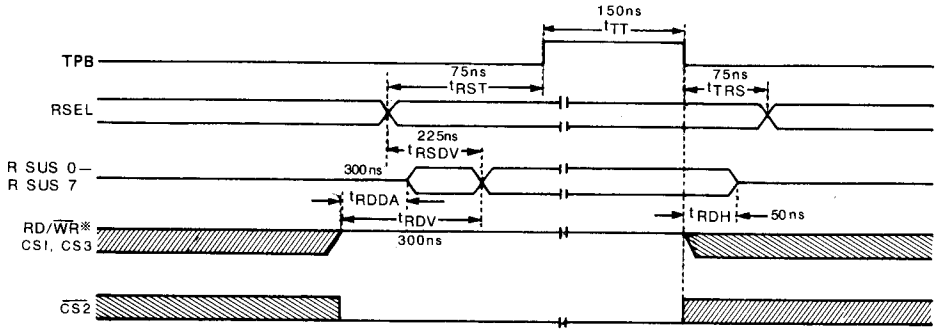
t OE AND PE ARE TERMINAL 15 AND ARE ALSO AVAILABLE AS TWO SEPARATE BITS IN THE STATUS REGISTER.

DYNAMIC ELECTRICAL CHARACTERISTICS at T_A = −40 to +85°C, V_{DD} ±5 %, t_r, t_f = 20 ns, V_{IH} = 0.7 V_{DD}, V_{IL} = 0.3 V_{DD}, D_L = 100 pF. See Figures 5 and 6.

CHARACTERISTIC		V_{DD} (V)	LIMITS						UNITS
			CDP1854A			CDP1854AC			
			Min.	Typ. •	Max. ▲	Min.	Typ. •	Max. ▲	
Receiver Timing – MODE 1									
Minimum Clock Period	t_{CC}	5	–	250	310	–	250	310	ns
		10	–	125	155	–	–	–	
Minimum Pulse Width: Clock Low Level	t_{CL}	5	–	100	125	–	100	125	ns
		10	–	75	100	–	–	–	
Clock High Level	t_{CH}	5	–	100	125	–	100	125	ns
		10	–	75	100	–	–	–	
TPB	t_{TT}	5	–	100	150	–	100	150	ns
		10	–	50	75	–	–	–	
Minimum Setup Time: Data Start Bit to Clock	t_{DC}	5	–	100	150	–	100	150	ns
		10	–	50	75	–	–	–	
Propagation Delay Time: TPB to $\overline{\text{DATA AVAILABLE}}$	t_{TDA}	5	–	220	325	–	220	325	ns
		10	–	110	175	–	–	–	
Clock to $\overline{\text{DATA AVAILABLE}}$	t_{CDA}	5	–	220	325	–	220	325	ns
		10	–	110	175	–	–	–	
Clock to Overrun Error	t_{COE}	5	–	210	300	–	210	300	ns
		10	–	105	150	–	–	–	
Clock to Parity Error	t_{CPE}	5	–	240	375	–	240	375	ns
		10	–	120	175	–	–	–	
Clock to Framing Error	t_{CFE}	5	–	200	300	–	200	300	ns
		10	–	100	150	–	–	–	
CPU Interface – READ Timing – MODE 1									
Minimum Pulse Width: TPB	t_{TT}	5	–	100	150	–	100	150	ns
		10	–	50	75	–	–	–	
Minimum Setup Time: RSEL to TPB	t_{RST}	5	–	50	75	–	50	75	ns
		10	–	25	40	–	–	–	
Minimum Hold Time: RSEL after TPB	t_{TRS}	5	–	50	75	–	50	75	ns
		10	–	25	40	–	–	–	
Read to Data Access Time	t_{RDDA}	5	–	200	300	–	200	300	ns
		10	–	100	150	–	–	–	
Read to Data Valid Time	t_{RDV}	5	–	200	300	–	200	300	ns
		10	–	100	150	–	–	–	
RSEL to Data Valid Time	t_{RSDV}	5	–	150	225	–	150	225	ns
		10	–	75	125	–	–	–	
Hold Time: Data after Read	t_{RDM}	5	50	150	–	50	150	–	ns
		10	25	75	–	–	–	–	

• Typical values are for T_A = 25°C and nominal voltages.

▲ Maximum limits of minimum characteristics are the values above which all devices function.



* READ IS THE OVERLAP OF CS1, CS3, RD/$\overline{WR}$ = 1 AND CS2 = 0.

Figure 6. MODE 1 CPU Interface (READ) Timing Diagram

Table 2. Interrupt Set and Reset Conditions

SET* ($\overline{INT}$ = LOW)	RESET ($\overline{INT}$ = HIGH)	
CAUSE	CONDITION	TIME
DA (Receipt of data)	Read of data	TPB leading edge
THRE ▲ (Ability to reload)	Read of status or write of character	TPB leading edge
THRE · TSRE (Transmitter done)	Read of status or write of character	TPB leading edge
$\overline{PSI}$ (Negative edge)	Read of status	TPB trailing edge
$\overline{CTS}$ (Positive edge when $\overline{THRE \cdot TSRE}$)	Read of status	TPB leading edge

- Interrupts will occur only after the IE bit in the Control Register (see Figure 3) has been set.

▲ THRE will cause an interrupt only after the TR bit in the Control Register (see Figure 3) has been set.

FUNCTIONAL DEFINITIONS FOR CDP1854A TERMINALS – CPD1802 and CDP1804 COMPATIBLE – MODE 1

SIGNAL: FUNCTION

V_{DD}:

Positive supply voltage.

MODE SELECT (MODE):

A high-level voltage at this input selects CDP1802 and CDP1804 Mode operation.

V_{SS}:

Ground

$\overline{CHIP\ SELECT\ 2}$ ($\overline{CS2}$):

A low-level voltage at this input together with CS1 and CS3 selects the CDP1854A UART.

RECEIVER BUS (R BUS 7 - R BUS 0):

Receiver parallel data outputs (may be externally connected to corresponding transmitter bus terminals). Not used on this model.

$\overline{INTERRUPT}$ ($\overline{INT}$):

A low-level voltage at this output indicates the presence of one or more of the interrupt conditions listed in Table 2.

FRAMING ERROR (FE):

A high-level voltage at this output indicates that the received character has no valid stop bit, i.e., the bit following the parity bit (if programmed) is not a high-level voltage. This output is updated each time a character is transferred to the Receiver Holding Register.

PARITY ERROR or OVERRUN ERROR (PE/OE):

A high-level voltage at this output indicates that either the PE or OE bit in the Status Register has been set (see Status Register Bit Assignment, Figure 4).

REGISTER SELECT (RSEL):

This input is used to choose either the Control/Status Register (high input) or the transmitter/receiver data registers (low input) according to the truth table in Table 1.

RECEIVER CLOCK (RCLOCK):

Clock input with a frequency 16 times the desired receiver shift rate.

TPB:

A positive input pulse used as a data load or reset strobe.

$\overline{\text{DATA AVAILABLE}}$ ($\overline{\text{DA}}$):

A low-level voltage at this output indicates that an entire character has been received and transferred to the Receiver Holding Register.

SERIAL DATA IN (SDI):

Serial data received on this input line enters the Receiver Shift Register at a point determined by the character length. A high-level input voltage must be present when data is not being received.

$\overline{\text{CLEAR}}$ ($\overline{\text{CLEAR}}$):

A low-level voltage at this input resets the Interrupt Flip-Flop, Receiver Holding Register, Control Register, and Status Register, and sets SERIAL DATA OUT (SDO) high.

$\overline{\text{TRANSMITTER HOLDING REGISTER EMPTY}}$ ($\overline{\text{THRE}}$):

A low-level voltage at this output indicates that the Transmitter Holding Register has transferred its contents to the Transmitter Shift Register and may be reloaded with a new character.

CHIP SELECT 1 (CS1):

A high-level voltage at this input together with $\overline{\text{CS2}}$ and CS3 selects the UART.

$\overline{\text{REQUEST TO SEND}}$ ($\overline{\text{RTS}}$):

This output signal tells the peripheral to get ready to receive data. $\overline{\text{CLEAR TO SEND}}$ ($\overline{\text{CTS}}$) is the response from the peripheral. $\overline{\text{RTS}}$ is set to a low-level voltage when data is latched in the Transmitter Holding Register or TR is set high, and is reset high when both the Transmitter Holding Register and Transmitter Shift Register are empty and TR is low.

SERIAL DATA OUTPUT (SDO):

The contents of the Transmitter Shift Register [start bit, data bits, parity bit, and stop bit(s)] are serially shifted out on this output. When no character is being transmitted, high level is maintained. Start of transmission is defined as the transition of the start bit from a high-level to a low-level output voltage.

TRANSMITTER BUS (T BUS 0 - T BUS 7):

Transmitter parallel data input. These may be externally connected to corresponding Receiver bus terminals. Not used on this model.

RD/$\overline{\text{WR}}$:

A low-level voltage at this input gates data from the transmitter bus to the Transmitter Holding Register or the Control Register, as chosen by register select. A high-level voltage gates data from the Receiver Holding Register or the Status Register, as chosen by register select, to the receiver bus.

CHIP SELECT 3 (CS3):

High-level voltage at this input,together with CS1 and $\overline{\text{CS2}}$ selects the UART.

$\overline{\text{PERIPHERAL STATUS INTERRUPT}}$ ($\overline{\text{PSI}}$):

A high-to-low transition on this input line sets a bit in the Status Register and causes an $\overline{\text{INTERRUPT}}$ ($\overline{\text{INT}}$ = low).

$\overline{\text{EXTERNAL STATUS}}$ ($\overline{\text{ES}}$):

A low-level voltage at this input sets a bit in the Status Register.

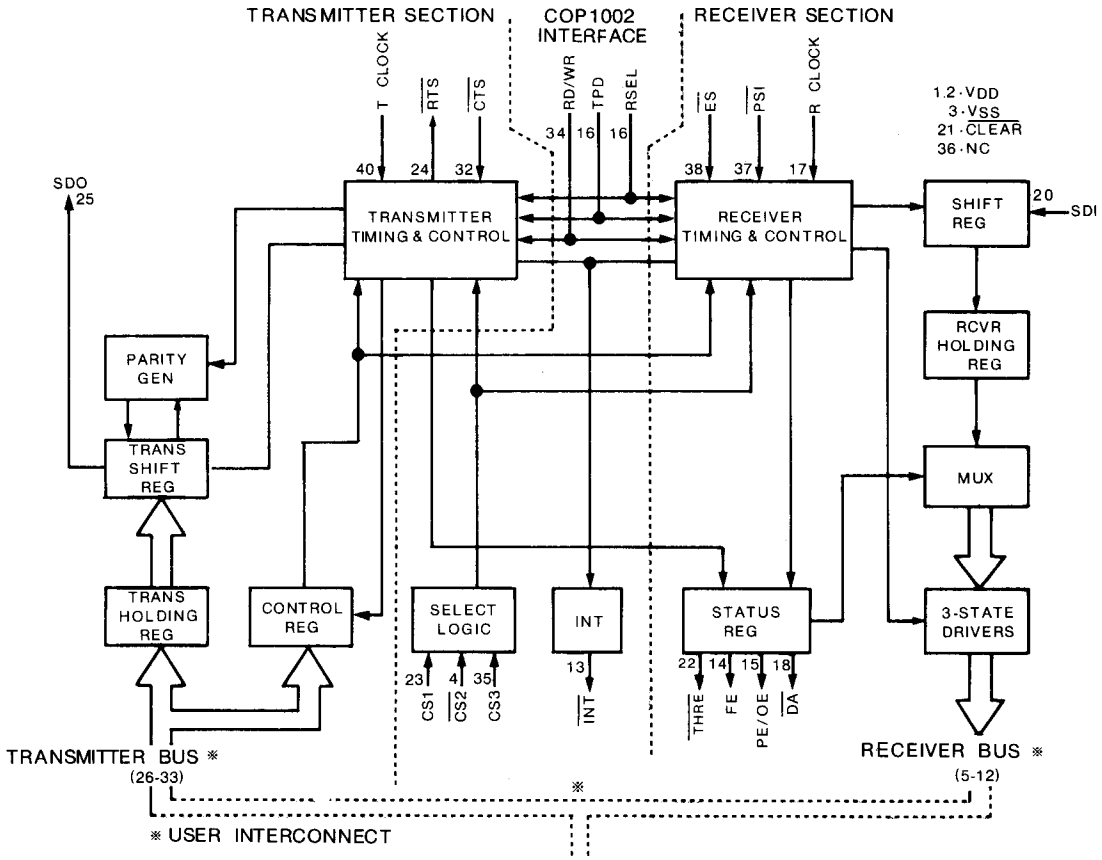
$\overline{\text{CLEAR TO SEND}}$ ($\overline{\text{CTS}}$):

When this input from a peripheral is high, transfer of a character to the Transmitter Shift Register and shifting of serial data out is inhibited.

TRANSMITTER CLOCK (TCLOCK):

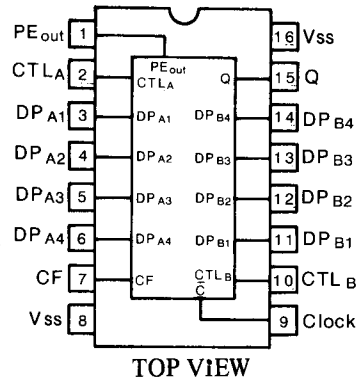
Clock input with a frequency 16 times the desired transmitter shift rate.

BLOCK DIAGRAM OF CDP1854A



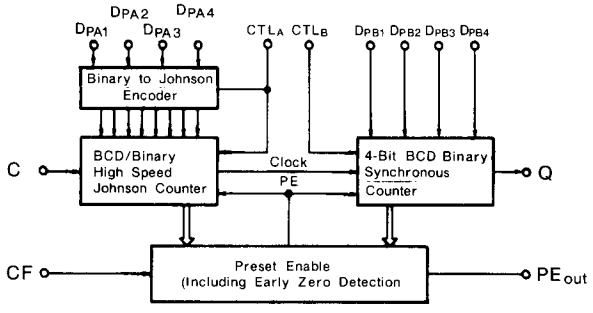
HD14569B

● PIN ARRANGEMENT



TOP VIEW

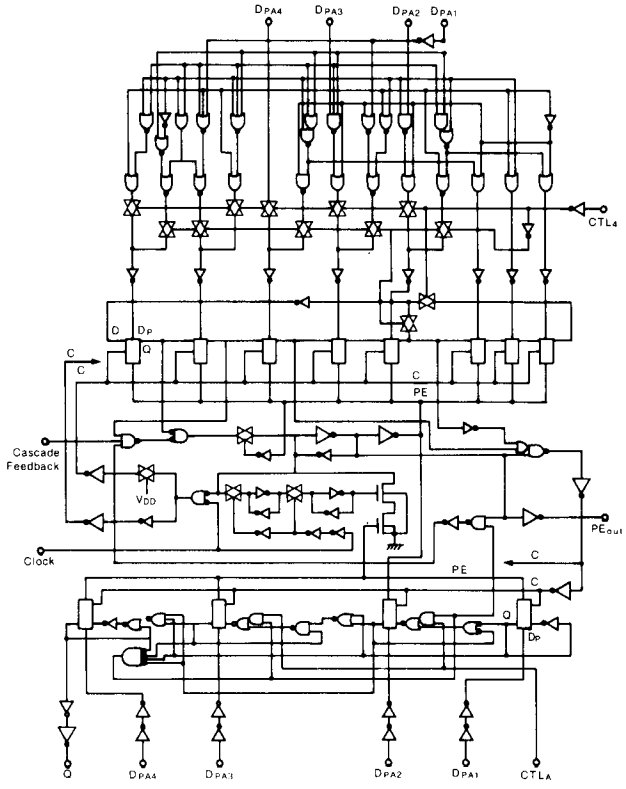
● BLOCK DIAGRAM



CTL = "0" AT BINARY COUNTING

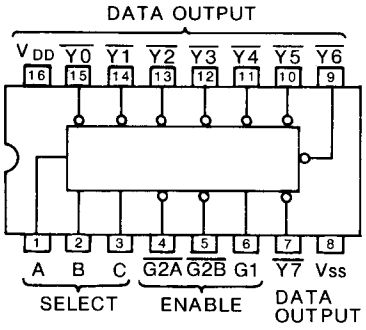
CTL = "1" AT BCD COUNTING

● LOG1C DIAGRAM

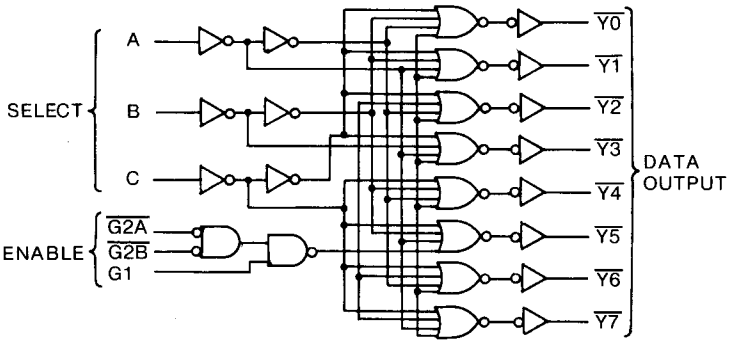


IC PIN CONNECTION

TC40H138P
Pin connections

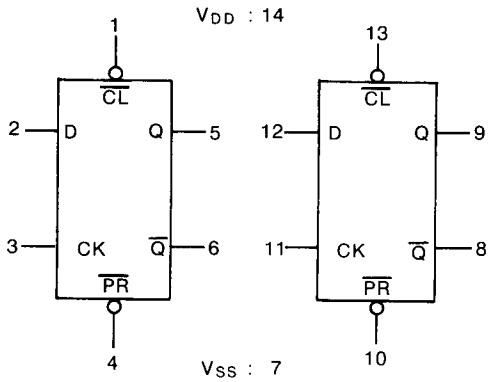


Logic diagram

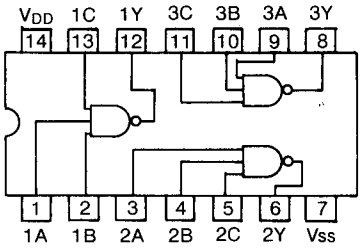


* Protective circuits provided for all inputs

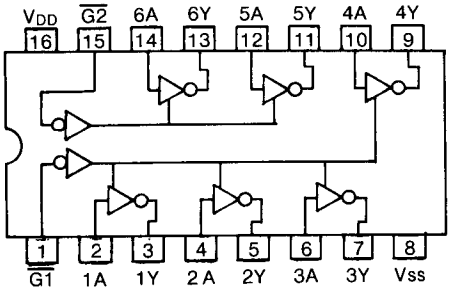
TC40H074P
Block diagram



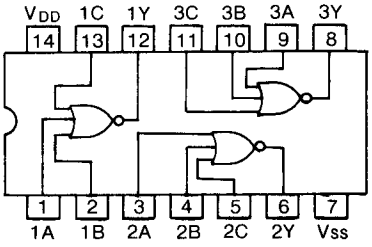
TC40H010P
Pin connections



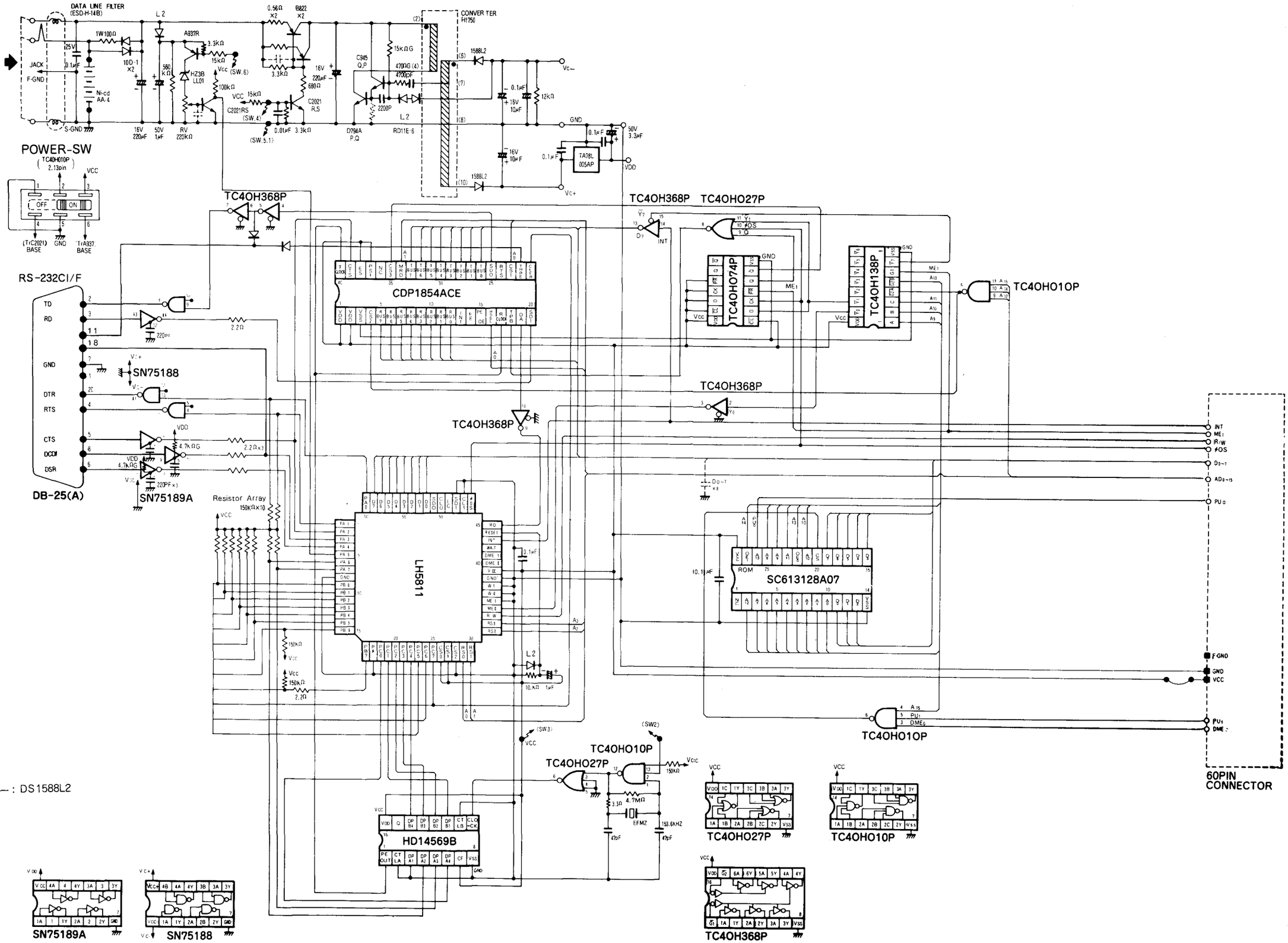
TC40H368P
Pin connections



TC40H027P
Pin connections



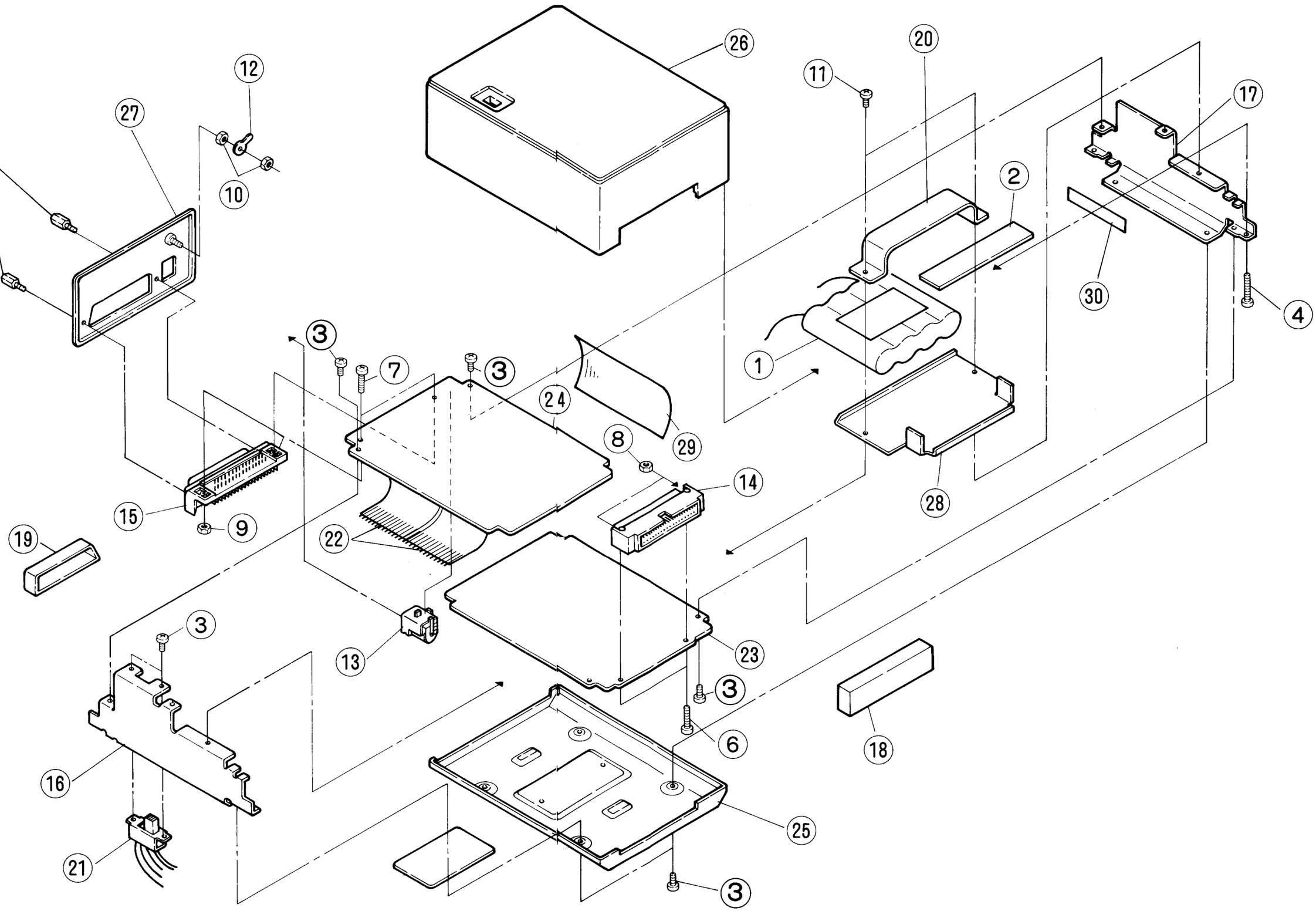
SCHEMATIC DIAGRAM



Note:

L2 : DS1588L2

EXPLODED VIEW



PARTS LIST

Ref. No.	Description	RS Part Number	Manufacturer Part Number
	Tr. 2SA937	AA-2SA937	VS2SA937-R/-1
	Tr. 2SB822	AA-2SB822	VS2SB822-//-1
	Tr. 2SC2021	AA-2SC2021	VS2SC2021-RSC
	Tr. 2SC945	AA-2SC945	VS2SC945-P/QC
	Tr. 2SD794A	AA-2SD794A	VS2SD794AP/QC
	Filter, Noise (EXT)	AC-0973	DUNT-7082CCZZ
	Filter, Noise	AC-0974	RFiLN1005CCZZ
	Capacitor, Ceramic, 0.01 μF, 50 V, 10 %	ACC-103KJCP	VCKYPU1HB103K
	Capacitor, Ceramic Semiconductor, 0.1 μF, 12 V, 20 %	ACC-104MDMP	VCTYPU1NX104M
	Capacitor, Ceramic Semiconductor, 0.1 μF, 25 V, 20 %	ACC-104MFMP	VCTYPU1EX104M
	Capacitor, Electrolytic, 1 μF, 50 V, 20 %	ACC-105MJAP	RC-EZ105ACC1H
	Capacitor, Electrolytic, 10 μF, 16 V, 20 %	ACC-106MDAP	RC-EZ106ACC1C
	Capacitor, Ceramic, 220 pF, 50 V, 10 %	ACC-221KJCP	VCKYPU1HB221K
	Capacitor, Ceramic, 2200 pF, 50 V, 10 %	ACC-222KJCP	VCKYPU1HB222K
	Capacitor, Electrolytic, 220 μF, 16 V, 20 %	ACC-227MDAP	RC-EZ227BCC1C
	Capacitor, Electrolytic, 3.3 μF, 50 V, 20 %	ACC-335MJAP	RC-EZ335ACC1H
	Capacitor, Ceramic, 47 pF, 50 V, 5 %	ACC-470JJCP	VCCCPU1HH470J
	Capacitor, Ceramic, 4700 pF, 50 V, 10 %	ACC-472KJCP	VCKYPU1HB472K
1	Battery, Ni-Cad pac	ACS-0098	CBATZ1054CC02
	Diode, DS1588	ADX-1304	VHDDS1588L2-1
	Diode, 10D1	ADX-1547	VHD10D1////-1
	Diode, Zener, HZ3BLL01	ADX-1548	VHEHZ3BLL01-1
	Diode, Zener, RD11E6	ADX-1844	VHERD11E6//-1
2	Cushion	AHC-2105	PCUSS1200CCZZ
	Cushion, IC	AHC-2106	PGUMS1450CCZZ
	Label, Caution	AHC-2107	TCAUH1201CCZZ
	Screw, M2 x 10, BLACK	AHD-2545	XBBSF20P10000
3	Screw, M2 x 4	AHD-2546	XBPSD20P04000
4	Screw, M2.6 x 6	AHD-2547	XUPSD26P06000
5	Screw, Special (MM screw)	AHD-2548	LX-BZ1135CCZZ
5	Screw, Special (Inch screw), USA/CANADA	AHD-2561	LX-BZ1141CCZZ
6	Screw, M2 x 10, YELLOW	AHD-2549	XBPSD20P10000
7	Screw, M2.6 x 8	AHD-2550	XBBSD26P08000
8	Nut, M2 x 1.6	AHD-7278	XNESD20-16000
9	Nut, M2.6 x 2	AHD-7279	XNESD26-20000
10	Nut, M3 x 2.4	AHD-7280	XNESD30-24000
11	Screw, M2 x 3		XBPSD20P03000
12	Lug	AHD-7281	QLUGE1080CCZZ
13	Socket, AC Adapter	AJ-7020	QJAKC1003CCZZ

Ref. No.	Description	RS Part Number	Manufacturer Part Number
14	Connector, Male, 60 P	AJ-7160	QCNCM1295CC6J
	Connector, Male, 2 P	AJ-7293	QCNCM1254CC0B
15	Connector, Female, 25 P	AJ-7294	QCNCW1305CC2F
	Socket, IC	AJ-7295	QSOCZTD28ACZZ
	Connector, Male, 5P	AJ-7296	QCNCM2331RC0E
	Connector, Female, 5 P	AJ-7297	QCNCW1311CC01
	Connector, Female, 2 P	AJ-7298	QCNCW1312CC01
	Crystal, 153·6 kHz	AMX-2992	RCRSZ1045CCZZ
	IC, SN75189A	AMX-4509	VHiSN75189A-1
	IC, LH5811	AMX-5070	VHiLH5811//-1
	IC, CDP1854ACE	AMX-5746	VHiCDP1854ACE
	LSI, SC613128P7	AMX-5747	VHiSC613128P7
	IC, TC40H010PN	AMX-5748	VHiTC40H010PN
	IC, TC40H027P1	AMX-5749	VHiTC40H027P1
	IC, TC40H074PN	AMX-5750	VHiTC40H074PN
	IC, TC40H138P1	AMX-5751	VHiTC40H138P1
	IC, TC40H368PN	AMX-5752	VHiTC40H368PN
	IC, HD14569B	AMX-5753	VHiHD14569B-1
	IC, SN75188N	AMX-5754	VHiSN75188N-1
	IC, TA78L005AP	AMX-5755	VHiTA78L005AP
	Resistor, Carbon, 0.56 OHM, 1/4 W, 5 %	AN-0013EEB	VRD-ST2EYR56J
	Resistor, Metal Oxide, 100 OHM, 1 W, 5 %	AN-0132EGD	VRS-PT3AB101J
	Resistor, Carbon, 470 OHM, 1/4 W, 2 %	AN-0169CEB	VRD-ST2EY471G
	Resistor, Carbon, 680 OHM, 1/4 W, 2 %	AN-0183EEB	VRD-ST2EY681J
	Resistor, Carbon, 2.2 k, 1/4 W, 5 %	AN-0216EEB	VRD-ST2EY222J
	Resistor, Carbon, 3.3 k, 1/4 W, 5 %	AN-0230EEB	VRD-ST2EY332J
	Resistor, Carbon, 4.7 k, 1/4 W, 2 %	AN-0247CEB	VRD-ST2EY472G
	Resistor, Carbon, 10 k, 1/4 W, 5 %	AN-0281EEB	VRD-ST2EY103J
	Resistor, Carbon, 12 k, 1/4 W, 5 %	AN-0288EEB	VRD-ST2EY123J
	Resistor, Carbon, 15 k, 1/4 W, 2 %	AN-0297CEB	VRD-ST2EY153G
	Resistor, Carbon, 15 k, 1/4 W, 5 %	AN-0297EEB	VRD-ST2EY153J
	Resistor, Carbon, 33 k, 1/4 W, 5 %	AN-0324EEB	VRD-ST2EY333J
	Resistor, Carbon, 100 k, 1/4 W, 5 %	AN-0371EEB	VRD-ST2EY104J
	Resistor, Carbon, 150 k, 1/4 W, 5 %	AN-0384EEB	VRD-ST2EY154J
	Resistor, Carbon, 560 k, 1/4 W, 5 %	AN-0429EEB	VRD-ST2EY564J
	Resistor, Carbon, 4.6 M, 1/4 W, 5 %	AN-0758EEB	VRD-ST2EY475J
	Resistor, Variable, 22 k	AP-7330	RVR-MB410QCZZ
16	Bracket, Left	ART-4753	LANGT1476CCZZ
17	Bracket, Right	ART-4754	LANGT1477CCZZ

Ref. No.	Description	RS Part Number	Manufacturer Part Number
18	Protection, Cap, 60 P, BLACK	ART-4755	PCAPH1013CCZZ
19	Protection, Cap, 25 P, RED	ART-4756	PCAPH1015CCZZ
	Holder panel for 26-3601	ART-4757	LHLDZ1181CCZZ
	Holder panel for 26-3605	ART-4758	LHLDZ1182CCZZ
20	Holder for fixing of Battery	ART-4759	LFiX-1144CCZZ
	Resistor, Block, 150 k x 10	ARX-0336	RMPTC0154QCKJ
21	Switch, Power	AS-2830	QSW-S1346CCZZ
	AC Adapter, USA/CANADA	ATA-1013	DUNT-3710CC02
	AC Adapter, Australlia		DUNT-3711CC02
	AC Adapter, U.K.		DUNT-3712CC02
	AC Adapter, Europe		DUNT-3713CC02
	Trans., Connector	ATA-1014	RTRNH1750CCZZ
22	Wire, Lead, FLAT	AW-3025	QCNW-1241CCZZ
23	PCB Assy (B), Lower	AX-9335	CPWBF2133CSNA
24	PCB Assy (A), Upper	AX-9336	CPWBF2133CSNB
25	Cabinet, Bottom	AZ-6862	GCABA2680CCZZ
26	Cabinet, Top	AZ-6863	GCABB2681CC01
27	Panel, Decoration	AZ-6864	HDECA2102CCZZ
28	Panel bottom for Battery	AZ-6865	LANGT1475CCZZ
	Template	AZ-6866	LPLTP1103CCZZ
29	Sheet, Insulator		PZETL1469CCZZ
30	Sheet, Insulator		PZETL1470CCZZ
	Sheet, Insulator		PZETL1172CCZZ

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