SHARP SERVICE MANUAL

CODE : 00ZPC1600SME2

MODEL PC-1600

This manual contents CE-1600P/CE-1600F/ CE-1600M/CE-1600L/CE-1601L/CE-1602L/ CE-1603L/CE-1604L

CONTENTS

SHARP CORPORATION

1. Scope

The PC-1600 has been designed with the following versatile features:

1. The most of PC-1500 BASIC software and the PC-1500 hardware options are compatible with the PC-1600.
2. Advanced technology gives the PC-1600 new features not available on the PC-1500.

1-1. Compatibility with the PC-1500 BASIC simulation mode

For compatibility with succeeding models, most of software created in BASIC for the PC-1500 can also run on the PC-1600.

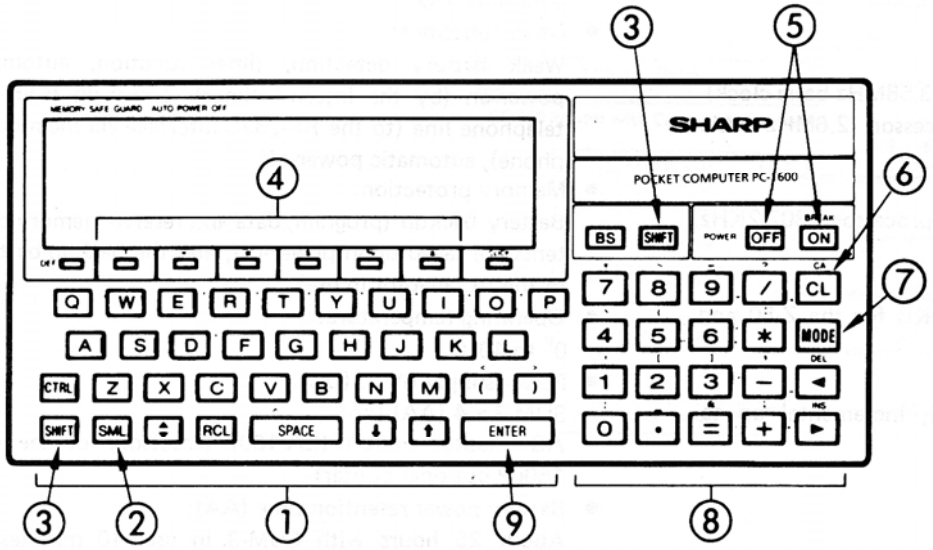
(a) For display in the simulation mode, a single line on the bottom of the display rows is subject for execution.
(b) In the simulation mode, the same character codes of the PC-1500 are used.
(c) The PC-1600 must work with a variety of PC-1500 software programs that include an option controlling system, and the PC-1600 system bus signals are upper grade compatible with the PC-1500 system bus. (Consideration is given for the use of the CE-150, 158, and 162E.)
(d) The slot signals are also upper grade compatible; this allows the use of the PC-1500 memory module on the PC-1600. (Memory modules usable: CE-151, 155, 159, and 161.) The CE-150 does not meet the upper grade compatibility test for software that uses the REM-1 because of a functional restriction on the PC-1600 optional printer CE-1600P, since the CE-150 has two data recorder remote control terminals (REM-0 and REM-1).

1-2. Implementation of functions that were not feasible with the PC-1500

(a) Adoption of a 26-digit by 4-line alphanumeric LCD unit.
(b) Operation speed of the PC-1600 is approx. 2.5 times faster than that of the PC-1500 as a result of using the general purpose microprocessor (Z-80) as the main CPU.
(c) Increased expansion module slot (two slots).
(d) Increased user memory area (11,834 Bytes user area out of 16KB basic RAM area).
(e) Implementation of the EIA, conforming to the internal RS-232C interface for communication.
(f) Implementation of the system wake-up (modem phone and timer started) and alarm functions.
(g) Adoption of the analog input, bar code reader input, and external keyboard input interface.
(h) Use of the internal optical fiber (SIO) interface.

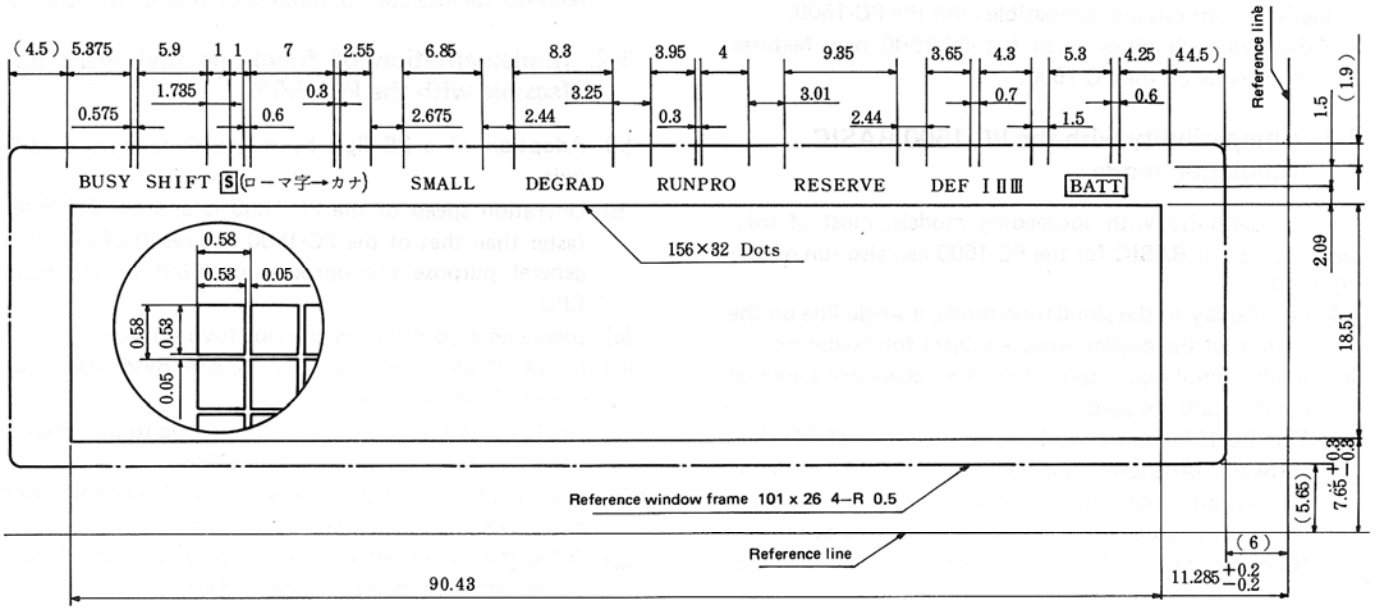
2. Specifications

- Model name: PC-1600
- Keyboard layout:



(1) Alphabetic keys
(2) Small key
(3) Shift key
(4) Function keys
(5) On and Off key
(6) Clear key
(7) Mode key
(8) Numeric and Arithmetic Operation keys
(9) Enter key

- Display unit:
  FEM-LCD (LF-7204E)
  Graphic display: 156 x 32 dots, 16 symbols
  Character display: 26 digits x 4 lines



Note 1 unit: mm

Fig. 1

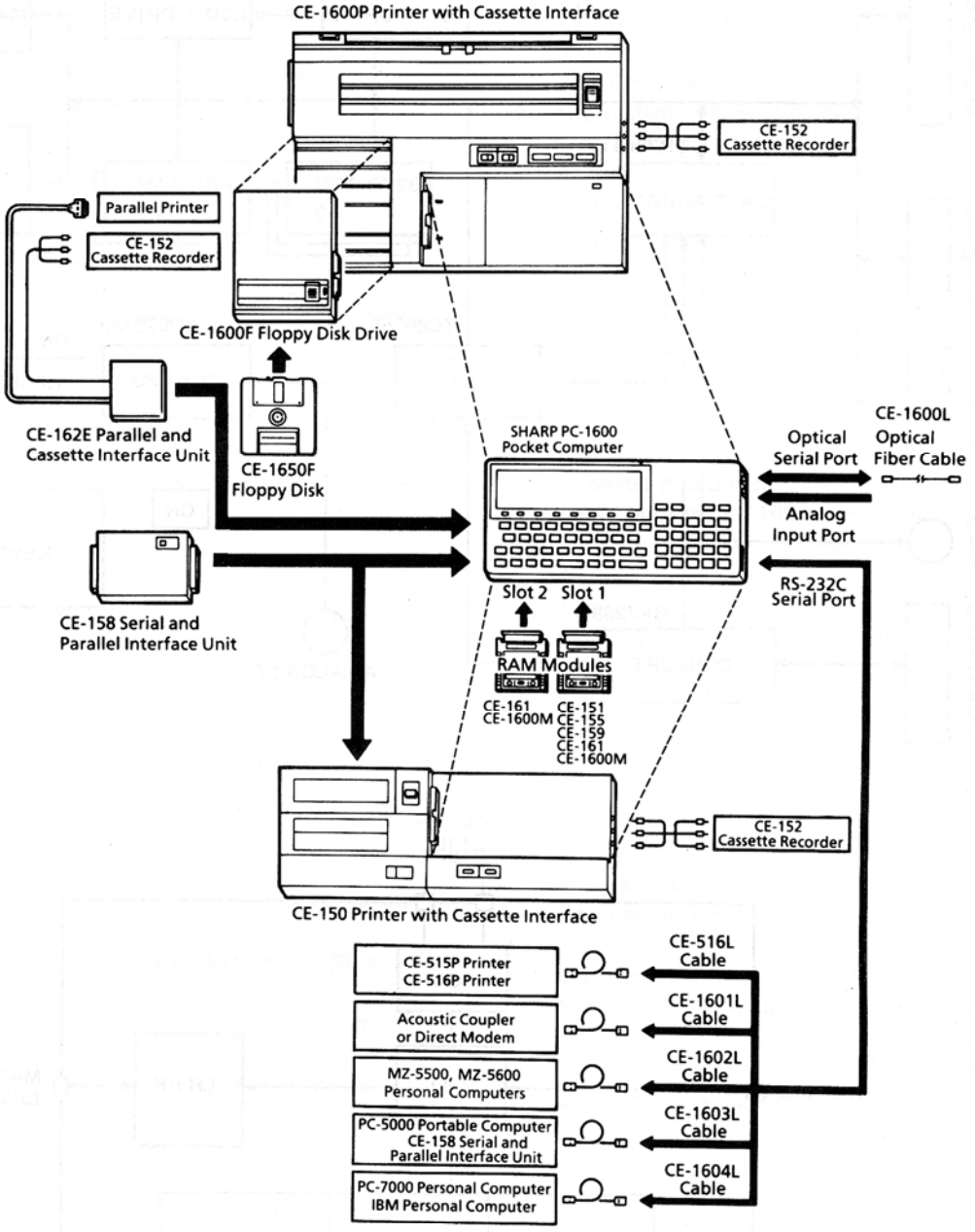
- Calculation capacity:
  10 digits (mantissa) + 2 digits (index)
- Calculation method:
  Formula based (with priority discrimination feature)
- Programming language:
  BASIC (PC-1500 upper grade compatible)
- Internal system configuration:
  Main CPU:
  - SC7852 (CMOS, Z-80 compatible, 3.58MHz basic clock)
  - LH5803 (CMOS, 8-bit microprocessor, 2.6MHz basic clock)

  Sub CPU:
  - LU57813P (CMOS, 4-bit microprocessor, 307.2KHz basic clock)

  ROM:
  - 96KB (BASIC interpreter) – (80KB for the Z-80 and 16KB for the LH-5803)
  - RAM:
  - 16KB (user area: 11,834 bytes), incremental up to 80KB.
- Basic calculation functions:
  Basic calculation:
  Four rules of math.
  Scientific calculation:
  Trigonometric function, inverse trigonometric function, logarithm, exponential, angular conversion, power raising, square root, integral, absolute value, signum, circle ratio.
- Edit functions:
  Horizontal cursor movement control (▶, ◀, CTRL + character key)
  Insertion (INS), deletion (DEL, CTRL + character key)
  Line up and down (↓, ↑)
- Interrupts:
  Timer interrupt, RS-232C interface interrupt, analog input interrupt, function key interrupt
- Interfaces:
  RS-232C interface, optical SIO interface, analog signal input interface
- Other functions:
  Weak battery detection, timer function, automatic power-on (by the internal timer), power-on from the telephone line (to the RS-232C interface via the modem phone), automatic power-off
- Memory protection:
  Battery backup (program, data and reserve memory contents are saved upon power-off, and the backup battery of the AC adaptor in use)
- Operating temperature:
  0° to 40°C
- Power supply 6V ... (DC):
  SUM-3 x 4 (AA) (x4)
  AC adaptor option (EA-160) (accessory of the CE-1600P optional printer)
- Battery power retention time (AA):
  About 25 hours with SUM-3 in use; 10 minutes of operation or program execution and 50 minutes of data on display per hour under the operating temperature of 20°C.
- It may vary depending on the kind of battery and use.
- Power consumption:
  0.48W
- Physical dimensions:
  195mm (W) x 86mm (D) x 25.5mm (H)
- Weight:
  375g (including batteries)

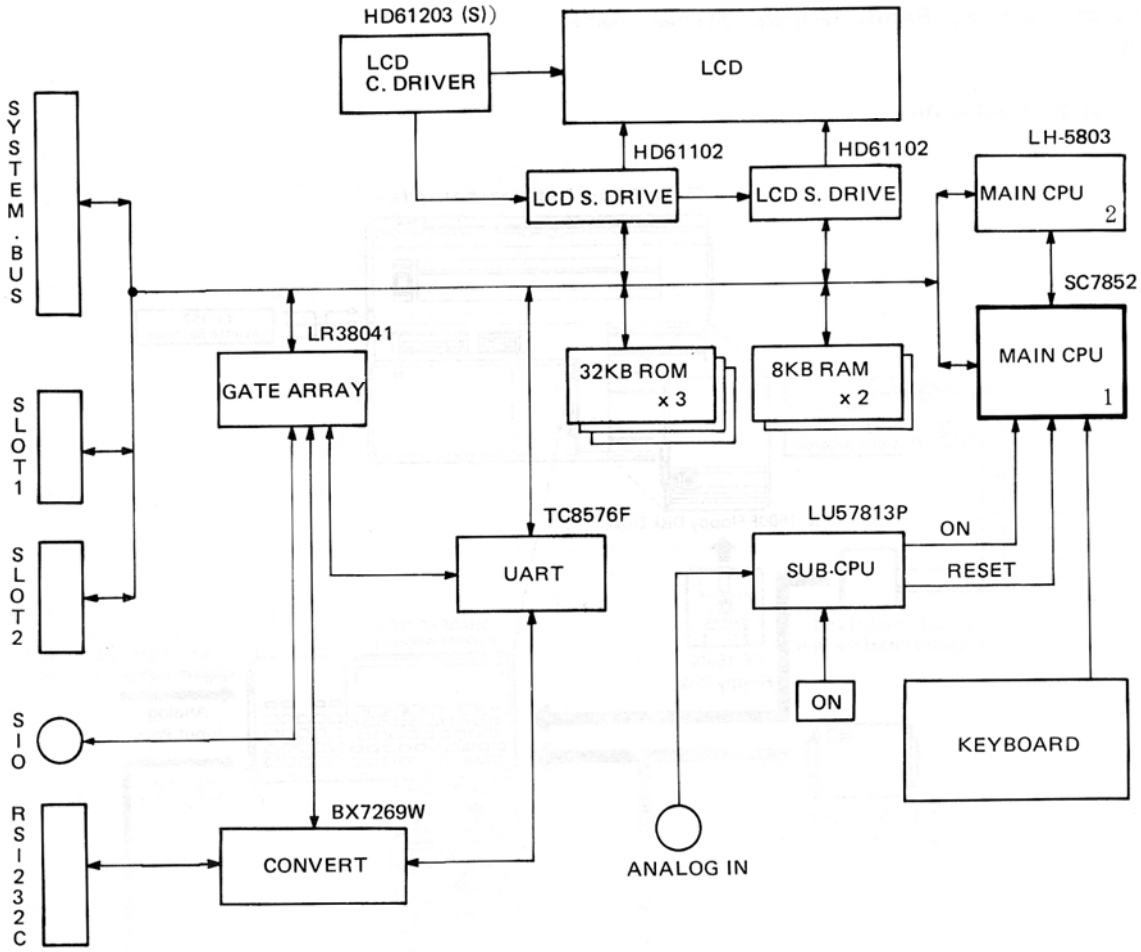
- Accessories:
  Soft case, template (x 1), SUM-3 batteries (AA) (x 4), instruction manual, BASIC language manual, name label

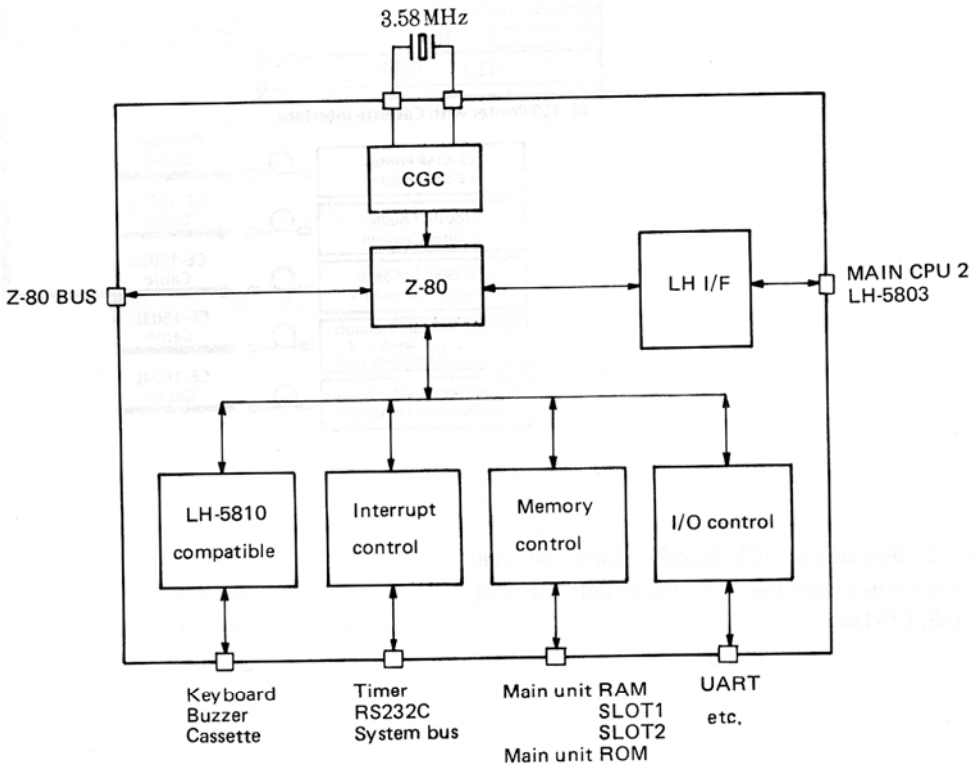
3. System configuration



NOTE: The PC-1600 option (CE-1600P) cannot be used in conjunction with the PC-1500 option (CE-150, CE-158, CE-162).

4. PC-1600 block diagram





Main CPU internal block diagram

Fig. 2

4-1. Relation of the main CPU-1 to the main CPU-2

Since two CPUs are linked together, the bus line of one CPU is on the sytem bus; the other CPU bus is kept in the floating state.
Shown in the following table are the bus signals of the two CPUs in connection.

SC7852 signal name	Z-80 signal name	LH-5803 signal name
A15 ~ A0	A15 ~ A0	A15 ~ A0
DB7 ~ DB0	D7 ~ D0	D7 ~ D0
MREQ	Opposite polarity of $\overline{\text{MREQ}}$	ME0
IORQ	Opposite polarity of $\overline{\text{IORQ}}$	ME1
$\overline{\text{RD}}$	$\overline{\text{RD}}$	OD*
$\overline{\text{WR}}$	$\overline{\text{WR}}$	R/$\overline{\text{W}}$

* The OD output of the LH-5803 is connected to $\overline{\text{RD}}$ of the SC7852 via the gate array (LR38041).

The operating CPU is indicated by the $\overline{\text{ELH}}$ signal.
$\overline{\text{ELH}}$ = Low: LH-5803
$\overline{\text{ELH}}$ = High: Z-80

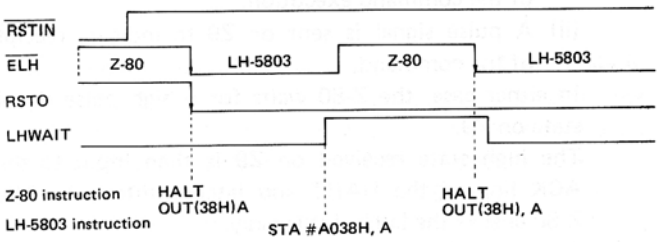


Fig. 3

The following takes place when a reset is applied to the SC7852 ($\overline{\text{RSTIN}}$ = Low).

① $\overline{\text{ELH}}$ goes to high to indicate that the Z-80 is in operation. At the same time, a reset is applied to the LH-5803. This allows the Z-80 to operate after the completion of the reset.

② With the following instruction, the Z-80 hands down the control to the LH-5803.
OUT(38H), A ···· A is don't care.
HALT
After the execution of the above instruction, the Z-80 bus is set in the floating state. At the same time, $\overline{\text{ELH}}$ goes to low along with RSTO, and the reset is cleared to the LH-5803 to start its operation.

③ With the following instruction, the LH-5803 hands down the control to the Z-80.
STA #A038H
A wait is applied to the LH-5803 (LHWAIT=High) to stop the operation of the LH-5803. When $\overline{\text{ELH}}$ goes to high, the LH-5803 bus is set in the floating state. With this, the Z-80 starts to operate.

④ In order that the Z-80 may hand down the control to the LH-5803, the Z-80 stops after the operation as in step 2 and the Z-80 bus is set in the floating state. Then, $\overline{\text{ELH}}$ goes to a low level so that the LH-5803 bus is activated. LHWAIT now goes to low which causes the LH-5803 to operate.

4-2. Sub CPU role

The sub CPU has the following roles.

(1) Main power-on and main power-off
① When the system-off command is received from the main CPU, the system is turned off.
② The system is turned on when the system is switched on by the [ON] key.

(2) Real timer
① Similar to the PC-1500; month, day, hours, minutes, and seconds are controlled by the PC-1600, though a leap year is not issued.
② A single wake-up timer and two alarm timers (incremented at every 0.5 second) are controlled.

(3) Weak battery detection
A weak battery condition is monitored by the A/D converter function held by the sub CPU.
① The level of the PC-1600 main power supply is checked.
② Also, the level of the power supply to the PC-1600 option is checked.
When it drops below the given level, the symbol [BATT] is activated on the LCD. When the hardware-monitored weak battery signal is turned to high, the system is then turned off.

(4) Analog input
The level of the input signal received through the PC-1600 analog input jack is A/D converted and returned to the main CPU.
Also, an external keyboard input through the same jack may be read and returned to the main CPU.

(5) Click sound
A click sound feature is supported by the PC-1600. When a keyboard entry is sensed in the click generate mode, the command is issued from the main CPU to generate a click sound.

(6) Reset signal
Two reset signal input lines are supported. When a signal is received on either line, a reset is applied to the system for the prescribed time (30 milliseconds).
① RESET switch on the back of the PC-1600
② RESET switch on the back of the CE-1600P

(7) System-on function with the CI signal of the RS-232C interface (checked at every 0.5 second)

(8) Timer signal output (1/64 sec.)

4-3. Sub CPU operation (Interfacing with the main CPU)

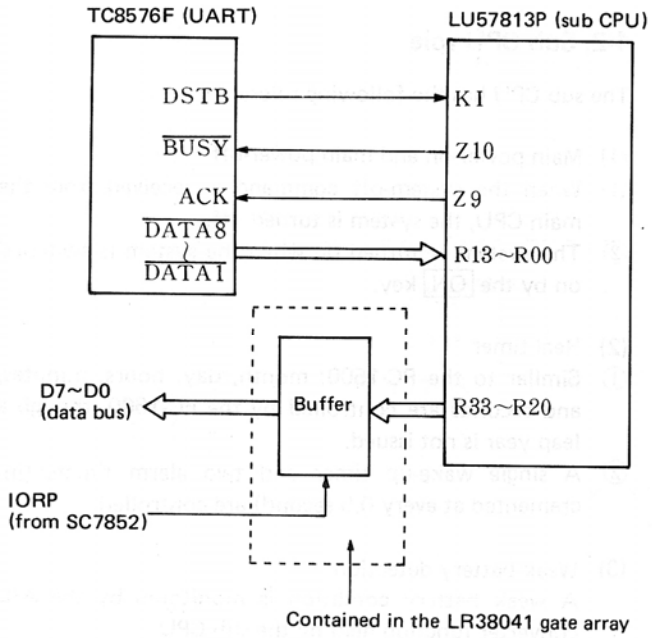
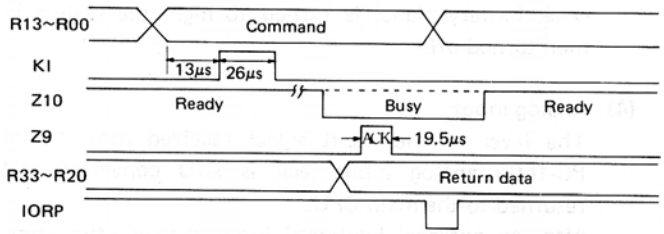
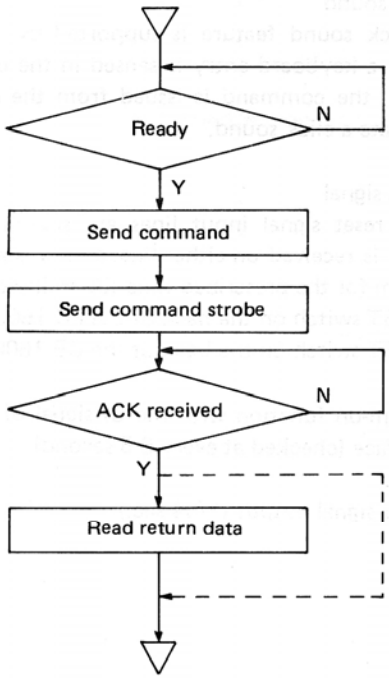


Fig. 4

Signals interfaced with the main CPU are KI, Z10, Z9, R13~R00, and R33~R20.



The following shows signal timings.



① Before the Z-80 CPU sends a command to the sub CPU, the sub CPU is asked if it is ready to receive the command. If it is not, the Z-80 waits until the sub CPU becomes ready.
The Z-80 assumes the sub CPU to be ready if the $\overline{\text{BUSY}}$ input of the UART is high.

② Next, 8-bit command data are sent to the sub CPU. The Z-80 sends the data on the DATA1~DATA8 port of the UART, which are received by the sub CPU through R13~R00. Unless ACK is returned within one second, the Z-80 proceeds to the next processing.

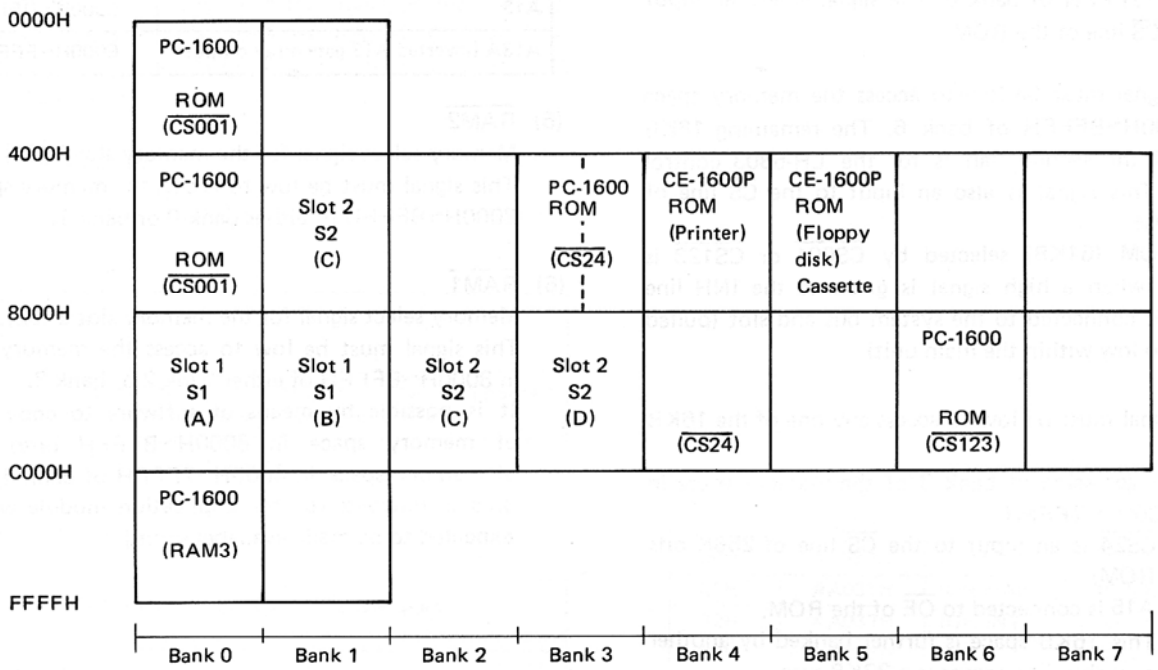
③ The Z-80 sends a pulse signal on DSTB of the UART in order to inform the sub CPU a command request, which the sub CPU receives of through the KI line.
With the KI line of the sub CPU high, an interrupt is sent to the sub CPU, and the command is processed in the interrupt service routine.

④ One of the following requests may be made depending on the command issued from the Z-80.
(i) A request for return data
(ii) A request not to return data
The sub CPU then interprets the above to proceed to the next step.
(i) A pulse signal is sent on Z9 after sending the return data on R33~R20, to indicate completion of the command execution.
(ii) A pulse signal is sent on Z9 to indicate receipt of the command.
In either case, the Z-80 waits for a high pulse signal state on Z9.
The high state received on Z9 is then input to the ACK line of the UART and latched internally. The Z-80 checks the latch if it is okay.

⑤ When the Z-80 accesses 33H of I/O to request the return data, it forces IORP to low so that the LR38041 gate array internal buffer is opened to send the return data (R33~R20) on the Z-80 bus D7~D0.

5. Memory mapping

5-1. Memory map as seen from the Z-80 (SC7852)



The memory space directly accessible by the Z-80 is 64KB, however, the memory space is expanded to 320KB for the PC-1600 by means of bank selection. Bank selection is done according to the contents of the Z-80 I/F address 31H.

When the Z-80 accesses a space in 000H~3FFFH, bank 0 or bank 1 is selected depending on the status in bit 0 (b0) of the I/O address 31H.

If b0 = 0, bank 0 → PVOUT: 0

If b0 = 1, bank 1 → PVOUT: 1

PVOUT (SC7852 output) is used to represent the chosen bank (0 or 1). PVOUT is 0 when bank 0 is selected. It is 1 when bank 1 is selected.

Similarly, when the Z-80 accesses a space in 4000H ~ 7FFFH, bank 0 ~ bank 7 is selected depending on the status in the bits, b3 ~ b1. PVOUT, PU, and PT are used to represent bank 0 thru bank 7.

The PVOUT, PU, and PT conform to the I/O address 31H and the space accessed by the Z-80.

It is possible to sense the status of the I/O address 31H.

Table-2

Bank No.	Z-80 accessing space	Status in the I/O address 31H								PT	PU	PV OUT	
		b7	b6	b5	b4	b3	b2	b1	b0				
0	0000H~3FFFH	*	*	*	*	*	*	*	*	*	*	0	
1	↑	*	*	*	*	*	*	*	1	*	*	1	
0	4000H~7FFFH	*	*	*	*	0	0	0	*	0	0	0	
1	↑	*	*	*	*	0	0	1	*	0	0	1	
2	↑	*	*	*	*	0	1	0	*	0	1	0	
3	↑	*	*	*	*	0	1	1	*	0	1	1	
C	↑	*	*	*	*	1	0	0	*	1	0	0	
5	↑	*	*	*	*	1	0	1	*	1	0	1	
6	↑	*	*	*	*	1	1	0	*	1	1	0	
7	↑	*	*	*	*	1	1	1	*	1	1	1	
0	8000H~BFFFH	*	0	0	0	*	*	*	*	0	0	0	
1	↑	*	0	0	1	*	*	*	*	0	0	1	
2	↑	*	0	1	0	*	*	*	*	0	1	0	
3	↑	*	0	1	1	*	*	*	*	0	1	1	
C	↑	*	1	0	0	*	*	*	*	1	0	0	
5	↑	*	1	0	1	*	*	*	*	1	0	1	
6	↑	*	1	1	0	*	*	*	*	1	1	0	
7	↑	*	1	1	1	*	*	*	*	1	1	0	
0	C000H~FFFFH	0	*	*	*	*	*	*	*	*	*	0	
1	↑	1	*	*	*	*	*	*	*	*	*	1	

*: DON'T CARE

5-2. Chip select signal

(1) $\overline{CS001}$
This signal must be low to access the memory space in 0000H~7FFFH of bank 0. The signal is also an input to the $\overline{CS}$ line of the ROM.

(2) $\overline{CS123}$
This signal must be low to access the memory space of 8000H~BFFFH of bank 6. The remaining 16KB area of the second half is for the LH-5803 control ROM. This signal is also an input to the $\overline{CS}$ line of the ROM.
The ROM (64KB) selected by $\overline{CS001}$ or $\overline{CS123}$ is cleared when a high signal is given to the INH line which is connected to the system bus and slot (pulled down to low within the main unit).

(3) $\overline{CS24}$
This signal must be low to access any one of the 16KB spaces.
(a) For accessing of bank 3 of the memory space in 4000H ~ 7FFFH.
- $\overline{CS24}$ is an input to the $\overline{CS}$ line of 256K bits ROM.
- A15 is connected to $\overline{OE}$ of the ROM.
- This 16KB space is further banked by another port signal to compose a 32KB area.

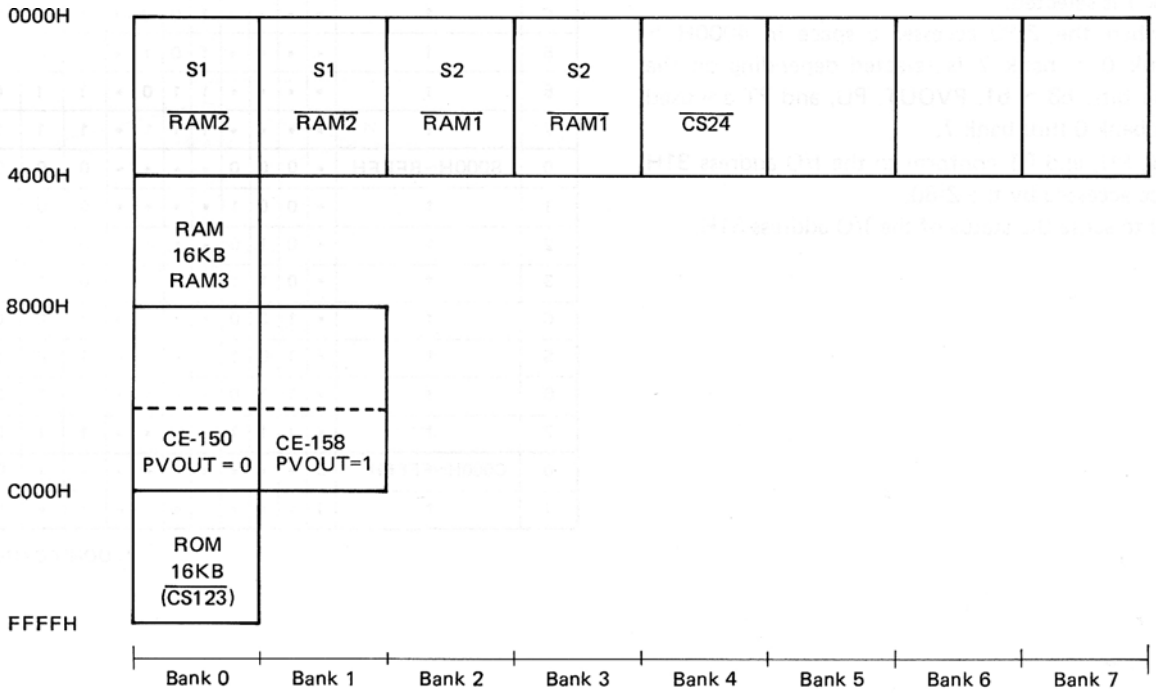
(4) RAM3
This signal must be high to access the memory space in C000H~FFFFH of bank 0. This signal is connected to CE2 of the two 8KB RAMs. A13 is used to determine which RAM is to be selected.

8KB RAM $\overline{CE1}$ input	Memory space chosen
A13	C000H~DFFFH
A13A (inverted A13 gate array output)	E000H~FFFFH

(5) $\overline{RAM2}$
Memory select signal for the memory slot 1 (S1).
This signal must be low to access the memory space in 8000H~BFFFH of either bank 0 or bank 1.
1.

(6) $\overline{RAM1}$
Memory select signal for the memory slot 2 (S2).
This signal must be low to access the memory space in 8000H~BFFFH of either bank 2 or bank 3.
It is possible by means of software to copy 16KB of memory space in 8000H~BFFFH onto 16KB of memory space in 4000H~7FFFH of bank 1. (This area is reserved for the application module which is expected to be made availabel soon.)

5-3. Memory map as seen from the LH-5803



(1) The memory space in 0000H~3FFFH is the same as the memory space in 8000H~BFFFH of the Z-80. The method of accessing is also the same.
(2) The memory space in 8000H~FFFFH is the same as that in the PC-1500. The PV signal of the LH-5803 is used to select the bank for 8000H~BFFFH. (The PV signal of the LH-5803 is directly sent by PVOUT of the SC7852.)

5-4. I/O mapping

The I/O space of the Z-80 consists of 256 bytes in 00H~FFH.

00H 0FH	Use prohibited.
10H 1FH	Port corresponding to LH-5810 (LH-5811) contained in the SC7852 (not synchronized with ϕOS).
20H 27H	TC8576F UART selection
28H 2FH	S2 (slot 2)
30H 3FH	SC7852 internal LSI control register port
40H 4FH	System reserve
50H 58H	HD61202 (IC2), (IC3)
	HD61202 (IC3)
5BH	HD61202 (IC2)
	System reserve
60H 6FH	S2 (slot 2)
78H 7FH	CE-1600F
80H 83H	CE-1600P
84H F8H	

Z-80 I/O address	LH-5803 address	Read	Write
30H	#A030H	IOR MOD	IOW MOD
31H	#A031H	IOR MAP	IOW MAP
32H	#A032H	IOR INT	IOW PRI
33H	#A033H	IOR P	IOW CDF
34H	#A034H	IOR LHMSK	IOW LHMSK
35H	#A035H	IOR ZMSK	IOW ZMSK
36H	#A036H	IOR ADRS	IOW CL1
37H	#A037H	IOR KB	IOW CGC CGC register write
38H	#A038H		IOW STP
39H	#A039H		IOW VCT
3AH	#A03AH		IOW KA Not used
3BH	#A03BH		IOW KS Not used
3CH	#A03CH		IOW SLT
3DH	#A03DH		IOW C/D
3EH	#A03EH		
3FH	#A03FH		

NOTES:
(Rreg): Indicates the contents of the memory (ME1 accessed) which are implied by the LH-5803 CPU internal register (R register).
☐ : Vacancy in the Z-80 I/O map which is not used at present.

6. Power supply

6-1. Kinds of power supplies

Power supply	Voltage range	Description
VGG	4.0 ~ 4.7V	• Logic driving power which is on while the system is not operating. Power is supplied to the chips that need protection. (1) RAM16KB Memory protection (2) LU57813P Real-time timer and wake-up timer protection (3) HD61102 Display data protection which is required to activate the display at power-on after auto power-off. (4) LR38041 To maintain the signal level of such as the memory select signal at a non-active level.
VCC	4.0 ~ 4.7V	• Logic driving power which is shut off when the system is turned off. Power is supplied to the chips that do not need protection when the system is off. (1) ROM 256Kbit (2) CPU SC7852, LH5803 (3) HD61203(S) LCD common driver chip (4) TC8576F UART LSI
VEE	Approx. −8.5V	• For creation of a low voltage to the LCD drive voltage and the RS-232C interface signals.
VDD	Approx 6.0V	• For creation of a high voltage to the RS-232C interface signals. This voltage, however, is supplied when PRIME is at a high level (RS-232C is chosen) and shut off when PRIME is a low level.

6-2. Power generation method

The following power supply sources are used to generate the above power requirements.

(1) Internal dry battery cells (x 4)
(2) Through the AC adaptor
(3) Supplied through the V_{BAT} of the system bus
A high voltage supply level is used by the PC-1600.
(i) VGG
A voltage of about 4.7V is normally supplied from the above source. The voltage drops when the level of power supply decreases.
(ii) VCC
VGG is supplied through this line, when BFO is at a low level or ACL is at a high level.
VCC is not supplied when the system is off.
(iii) VEE
VEE is supplied when the system is turned on.
(iv) VDD
VDD is supplied when the PRIME output is at a high level with the system on.

6-3. System-on/system-off

The on/off state of the system is controlled by the LU 57813P. The on/off state of the system is seen on the BFO output. When BFO is low, the system is on and VCC and VEE are available. When the system is off, no power is supplied except VGG.

(1) System-off to system-on
There are five ways.
(i) Use of the BREAK/ON key
(ii) By means of the wake-up function
Possible to disable with mask
(iii) By means of the RS-232C interfacing CI signal
(iv) Use of the ALL RESET switch (ACL signal) located on the back of the PC-1600
(v) By means of the reset input from the CE-1600P
Normally, the system is turned off with (i).
(2) System-on to system-off
There are two ways.
(i) By means of the Z-80 command
(ii) By means of the weak battery detect signal (Q3)

7. System operation

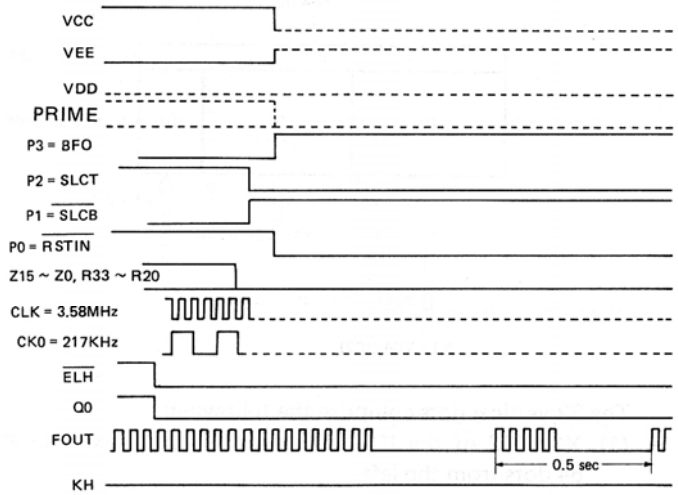
7-1. System-off operation

LSIs operated by VGG, except for the LU57813P, are assigned to protect their contents.
For the LU57813P, the real timer needs to be revised when the system is off. So, an interrupt is sent to the LU57813P by the internal timer every 0.5 second to revise the real timer. When seconds are carried to a minute, the time is verified with the wake-up timer and the alarm time. Therefore, a system clock (153.6KHz or 307.2KHz) is issued on FOUT of the LU57813P every 0.5 second.

The system starts to rise when Q1 of the CI connected subcontroller remains high for more than the predetermined time; the system wake-up is also possible by the CI input of the RS-232C interface which is input at 0.5 second intervals.
But, if the system is forced off because of a weak battery condition (Q3 input at high), the 0.5 second interval timer interrupt is not activated even if the weak battery condition is cleared.

	System-off (down) in the Q3 state	Normal system-off
1	The real-time timer is not revised.	A timer interrupt is issued every 0.5 second to revise the real-time timer.
2	FOUT is not issued.	FOUT is issued every 0.5 second.
3	The system can be turned on by one of the following operations after clearing the weak battery condition. ① Depression of the BREAK/ON key ② Depression of the ALL RESET switch located on the back of the PC-1600	The system can be turned on by one of the following operations. ① Depression of the BREAK/ON key ② Depression of the ALL RESET SWITCH located on the back of the PC-1600 ③ Depression of the RESET switch located on the back of the CE-1600P ④ When the wake-up time meets the real time as programmed by the WAKE$(0) statement ⑤ When the RS-232C interface CI input is set high by the WAKE$(1) statement

The figure below shows the timings when the system turns off.



① When the subcontroller receives the system-off command from the main CPU, it confirms that both Q0 and KH are at a low level. Then, P2 and SLCT are forced to low to disable the memory selection. If KH is at high, the control proceeds to the system in sequence.

② Then, P3 and BFO are set to high to turn off the system power supply. With this, all inputs and outputs of the SC7852 and LH-5803 are turned to a low or high impedance.

③ The subcontroller goes into the standby mode, but the real-timer issues a timer interrupt ever 0.5 second. second.

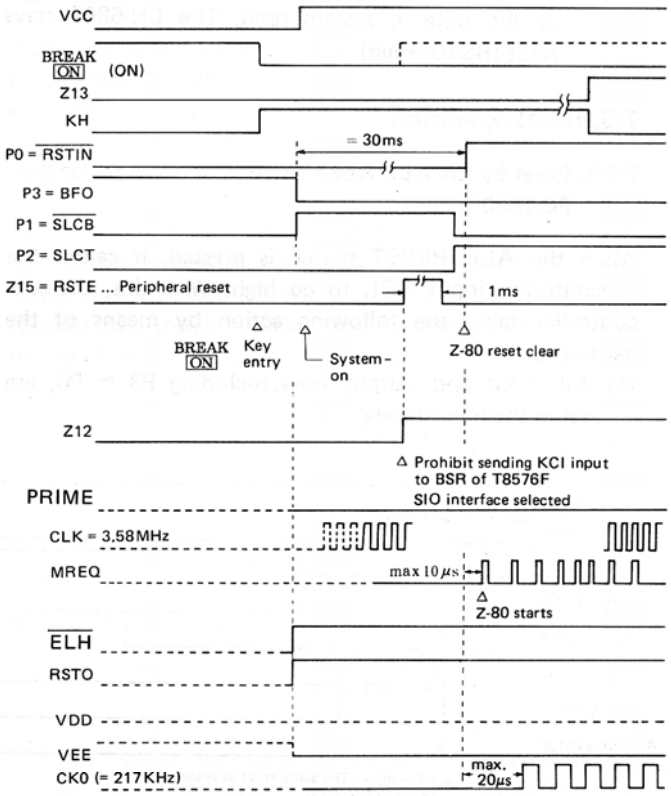
(a) If the wake-up timer has been set, the time on the real-timer is checked for whether it coincides with the wakeup time. If it coincides, the system is turned on.

(b) If the wake-up timer is set to turn on the system with the RS-232C interface CI input, the system is turned on with the input of the CI signal as it has been monitored.

If the weak battery signal Q3 goes high when the system is off, the system down is established.

7-2. System-on operation

The figure below shows the timing sequence when the system is turned on by the BREAK/ON key.



① When the BREAK/ON key is pushed while the system is off, the ON input of the LR38041 converts to low. As Z13 is low, KH goes high.

② When KH goes high, the subcontroller starts to operate assuming the start of the system. First, P3 is set low, P2 low, P1 high, and P0 low. Now, VCC is activated because P3 and BFO are low, and the system reset is applied with low P0 and $\overline{\text{RSTIN}}$ states. The memory and I/O selections are prohibited in low P2 and SLCT states.

③ Low P0 and $\overline{\text{RSTIN}}$ states are issued for 30 milliseconds.

④ The Z15 peripheral reset output is issued for 1 millisecond to reset peripherals.

⑤ First, P2 and SLCT are set to high to select memory and I/O, then the system reset is cleared.

⑥ In order to supply stable clocking to the Z-80, it takes about 0.3 millisecond before supplying the system clock.

⑦ After the system reset has been cleared, the Z-80 starts operation within 10 microseconds and the Z-80 begins to read the contents of the address 0000H. (MREQ issued)

⑧ Now, the Z-80 starts to supply clock pulse to the HD61203 LCD driver (217KHz on the CK0) to activate the LCD.

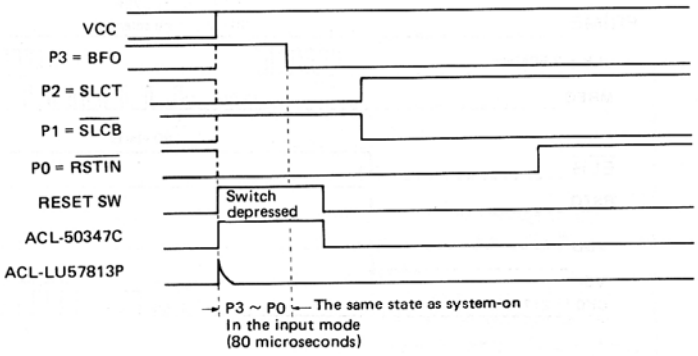
- The LCD voltage VEE is activated at the same time the system is turned on.
- Supply voltage VDD on the RS-232C high level side will be issued only when PRIM is at a high state. But, VDD is not supplied during power-on because PRIM is at a low level then.
- A high ELH state indicates that the Z-80 is started at the time of system reset. The LH-5803 stays reset (RST0=High).

7-3. Reset operation

7-3-1. Reset by the ALL RESET switch on the back of the PC-1600

When the ALL RESET switch is pressed, it causes the subcontroller input ACL to go high. With this, the subcontroller takes the following action by means of the hardware.

(1) All input and output lines, including P3 ~ P0, are set in the input mode.



① Regardless whether the system is turned on or off, P3~P0 are set in the input mode and are kept in the floating condition while the reset is applied to the subcontroller.
P3 is pulled up with the resistor.
P2 is pulled down with the resistor.
P1 is pulled up with the resistor.
P0 is pulled down with the resistor.
While P2~P0 are pulled down towards the non-active direction, P3 is pulled up towards the system-off. So, the system's power supply is turned off in those states. However, the power is supplied to the system while the RESET switch is in depression.

7-3-2. Reset by the RESET switch on the back of the CE-1600P

When the RESET switch on the back of the CE-1600P is pressed, KL and Z15 of the subcontroller go high. When this pulse width continues for more than 300 microseconds, the subcontroller proceeds in the same way as the system power-on procedure so that a reset is applied to the system.

7-3-3. Difference from ALL RESET

The subcontroller interrogates the state of the BREAK/ON key at 7-3-1 and 7-3-2 above in the following manner.

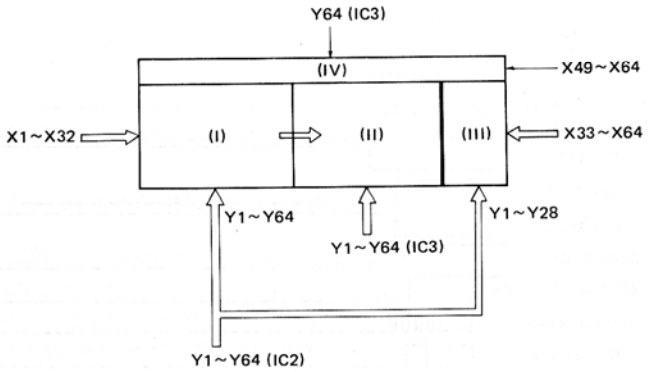
(1) If the BREAK/ON key is depressed, the all reset is assumed and all internals are intialized.

(2) If the BREAK/ON key is not depressed, the reset is assumed — the procedure to turn the system on from the system-off state. The internals are not initialized in this case.
It is possible to return reset from all reset by a request from the main CPU, the Z-80 asks the subcontroller for the cause when the reset is applied. Processing differs depending on the cause.
In the case of all reset ... Clears all memory contents.
In the case of reset ... Retains all memory contents.

7-4. LCD block

7-4-1. General

The LCD is 1/64 duty and consists of 156 x 32 dots and has 16 symbols.



The 32 vertical dots comprise the following:

(1) X1~X32 of the IC2 LCD driver outputs take care of 64 dots from the left.

(2) X1~X32 of the IC3 LCD driver outputs take care of 65~128 dots.

(3) X33~X64 of the IC2 LCD driver outputs take care of 129~156 dots in conjunction with Y1~Y28.

(4) X49~X64 take care of 16 symbol dots in conjunction with IC3 Y64.

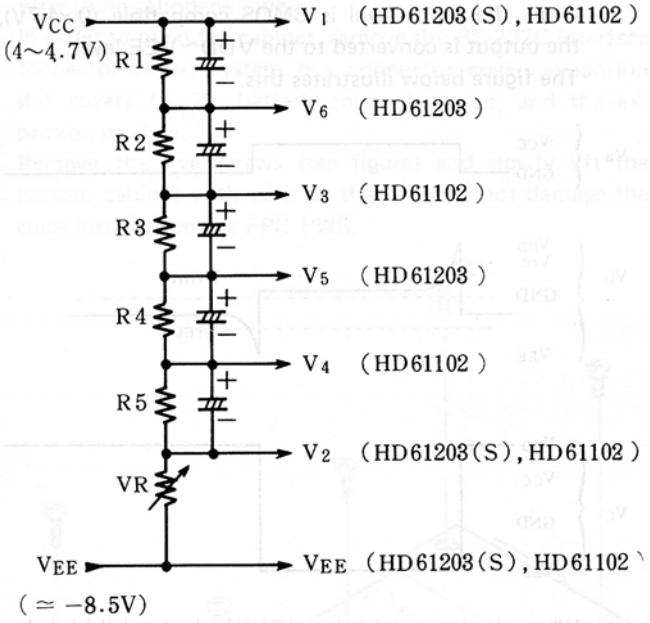
7-4-2. Operation

(1) The LCD driving basic clock (217KHz) supplied from CK0 of the SC7852 is connected to the LCD common driver. Without this signal, the LCD will burn out when a DC voltage is applied to the LCD.
This signal is issued only during the system-on time which appears immediately after the clearing of the reset. As it is in a low state during the reset, a DC voltage is added to the LCD during that period.

(2) The HD61202 LCD driver is for the 6800 series; the timing clock E required for this interface is sent from the SC7852.
The clock E goes high when the Z-80 accesses 40H~5FH of I/O. (It has a half clock delay against IORQ and its pulse width is 540 nanoseconds.)
But, the HD61102 will not be selected unless all three chip select lines ($\overline{CS1}$, $\overline{CS2}$, CS3) are enabled. Two HD61102s have the following address inputs as shown in the next table.

	HD61102 (IC2)	HD61102 (IC3)
$\overline{CS1}$	A2	A3
$\overline{CS2}$	A5	A5
CS3	A4	A4
Selected I/O space	50H ~ 53H 58H ~ 5BH	50H ~ 53H 54H ~ 57H

(3) For the LCD drive voltage, VCC−VEE are divided by a resistor to obtain the LCD drive voltages, V1~V6 and VEE.
VEE is derived from the power supply hybrid IC 50347C.



7-5. Keyboard block

7-5-1. Key scan timings

Keyboard key scan is done by a Z-80 interrupt with a 1/64 second timer interrupt (subcontroller output $\overline{INT4}$).

7-5-2. Method of scanning

Nine key strobe signals are obtained through PA7~PA0 and PB6 of the SC7852 I/O port.
Key scan is done in the following ways:

① Only the strobe signal of the Y row to be scanned is set low with other strobe signals set for the input mode.

② To scan another strobe row after the current strobing row, a high signal is issued to that strobing row first, then set in the input mode. So, a low signal is issued to PA7 ~ PA0 and PB6 at every 1/64 second to discriminate a key depression. In this instance, a low signal is sent to all strobe lines to sense a key depression. When a key depression is sensed, that particular key is distinguished after sending a strobe to each line.
As the key input appears on $\overline{KIN7}$~$\overline{KIN0}$ of the SC7852, a row of the keys in a low state is judged to be the row at which the key entry occurred. Since input not having a key entry is internally pulled up in the LSI, it is in a high level.

7-6. Buzzer block

7-6-1. General

These two lines activate the buzzer.

- PC6 output of the SC7852
- Subcontroller F output

7-6-2. Description

As the buzzer is sandwiched between two lines, oscillation from either line causes the buzzer to activate. Consumption current is 3 mA, maximum.
(Conditions: input voltage = 4.5Vp-p square wave, input frequency = 4.1KHz)

(1) PC6
The following three signal sources are connected to this line.

① PB2 ..... Cassette playback signal
② PC7 ..... Cassette recording signal and beep by a BEEP statement
③ SD0 ..... Recording signal by the CE-150 or CE-162E

But, when the beep is turned off, sound is not generated no matter what the above signals may be. The above three signal lines are normally high.

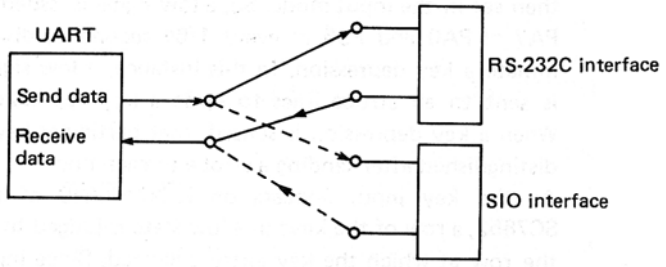
(2) F
The following three signal sources are connected to this line.

④ Click .... In the click mode, a click is generated each time a key is pushed.
⑤ Sound generated upon wake-up.
⑥ Sound generated before issuing an alarm message.

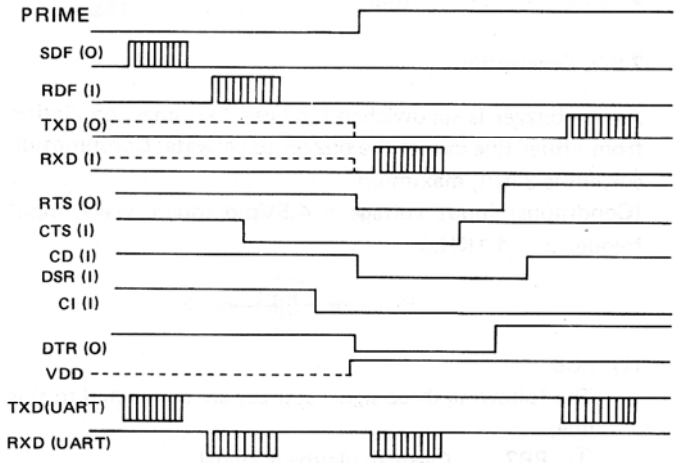
Normally, these three lines are low.

7-7. RS-232C interface and SIO interface

The following serial interfaces are provided for the PC-1600.
(1) RS-232C interface (COM1:)
(2) SIO interface (COM2:)
It incorporates the UART TC8576T as the hardware.
While the PC-1600 has two interfaces with single supported channel, only one interface can be active at one time. The OPEN or SETDEV statement is used to selectively activate the channel and the PRIME signal is used to activate the hardware.



At the same time the RS-232C interface is selected with a high PRIME state, VDD is supplied from the high side of the RS-232C interface.
The SIO interface is selected with a low PRIME state and VDD is turned off. During the system on and reset, PRIME is at low.

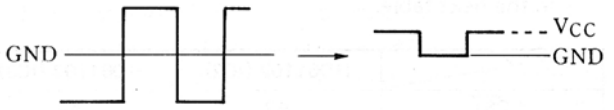


① When PRIME is at a low state, the RS-232C interface outputs either in a high impedance or a low state (non-active).
② When PRIME is at a low state, the SIO interface I/O signals, SDF and RDF, are in an opposite polarity with the UART input/output signals, TXD and RXD. The start bit is high and the stop bit is low. So, both are in a low state when no data are sent or received (UART TXD and RXD are at a high level).
③ When PRIME is at a high state, both SDF and RDF are at a low level and non-active (stop bit).
④ When PRIME is at a high state, TXD and RXD of the RS-232C interface are opposite in their polarity as are those of TXD and RXD of the UART.
⑤ When PRIME goes high, VDD is activated (RS-232C interface high side voltage).
⑥ The RS-232C interface input/output signals—CTS, DSR, CD, and CI—are input to the UART (opposite polarity), regardless of the state of PRIME (high or low).

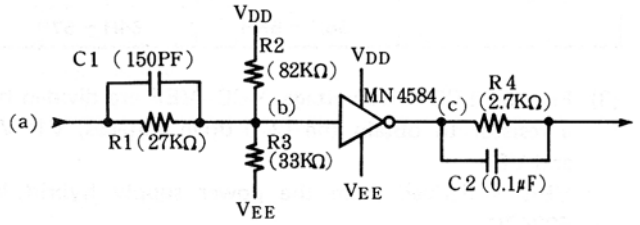
7-7-1. RS-232C interface signal

Although signals of this interface conform to the EIA standards, they are used for controls that differ in some ways from the RS-232C interface in general.

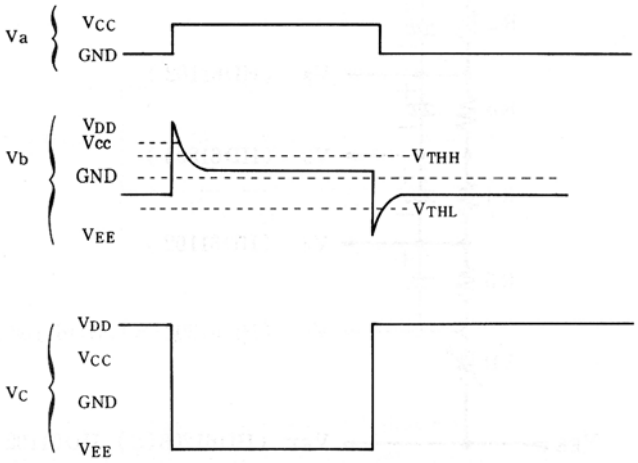
(1) Input signals are received by the transistor and are output through the open collector and pulled up to VCC using a resistor, as shown in the hybrid IC BX7269W. A diode is inserted across the base and emitter of the input which will bring the signal below the GND level (stop bit, etc.) and make it assume to be at the GND level. Therefore, the input signal is converted in the hybrid IC to be handled as a logic signal.



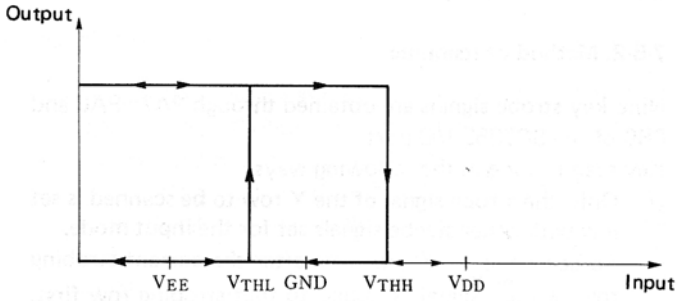
(2) On the other hand, the output signal is output through the circuit shown below (hybrid IC).



While the input level is CMOS compatible (0~4.7V), the output is converted to the VDD~VEE level.
The figure below illustrates this.



① When the input (a) is low (GND), the level (b) is below GND and is assumed by the MN4584 to be at a low level.
The MN4584 IC is a Schmitt inverter to which VDD and VEE is supplied. This IC has a hysteresis against input.



In order to change from high to low, the input must be above VTHH. On the other hand, for the output to turn from low to high, the input must be below VTHL. For the PC-1600, three resistors (R1, R2, R3) are chosen to for maintain (b) level is in between VTHH and VTHL under the normal state.

② When the input (a) changes from low to high, the signal (b) is sent to the VDD side as a pulse above VTHH by means of the capacitor C1 between VTHH and GND as a normal level. As a result, the signal (c) changes from high to low.

③ On the other hand, when input (a) changes from high to low, the signal (b) is sent to the VEE side as a pulse above VTHL by means of the capacitor C1 between VTHL and GND. As a result, the signal (c) changes from low to high.

A signal transition is latched on the output side using the pulse by means of the capacitor and characteristics of the Schmitt IC for conversion of a logic signal into the RS-232C interface signal.

The role of the R4 output is to prevent the possible destruction of the IC4584 which may occur by an accidental short in connection with the RS-232C interface or the connection of outputs together.

The capacitor C2 is for increasing speed for conveying a change in the MN4584.

8. Service precautions

Before servicing of the PC-1600, it is mandatory that you release static power in your body by using the earth band.
(When removing the key PWB from the top cabinet, it is recommended that you secure the keytops and display filter using cellopane tape.)

In order to open the cabinet, remove the RS-232C interface connector cover, system bus connector cover, expansion slot covers (1, 2), battery cover, batteries, and the expansion module.

Remove the five screws (see figure) and slowly lift the bottom cabinet with care so that you do not damage the chips installed on the FPC PWB.

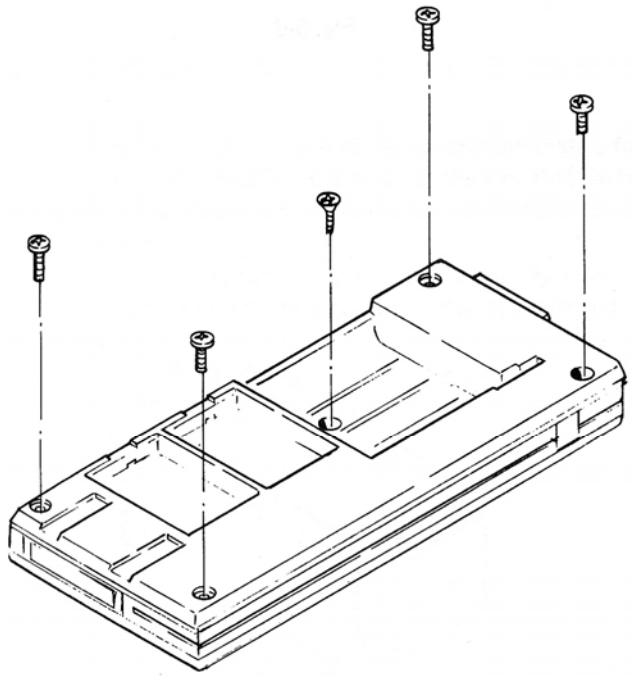


Fig. 8-1

Now, you will see the signal levels. To get power by using the AC adaptor or battery cells, connect the oscilloscope probe to the negative side of the battery.

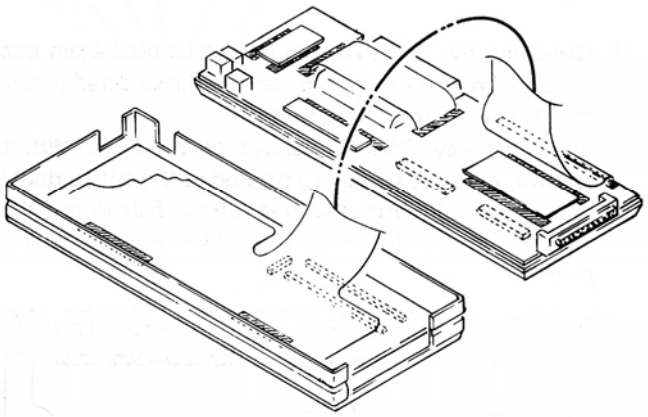


Fig. 8-2

8-1. Replacing the FPC PWB

1. With the connector PWB secured on the bottom cabinet, pry the holder (A) at (A) using a flat tip screwdriver. Next, remove the holder (B).

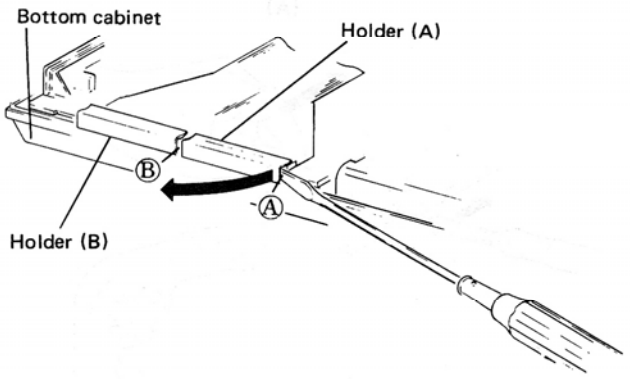


Fig. 8-3

2. Remove the eleven screws (see figure) and remove the key PWB (with the FPC PWB) from the top cabinet.

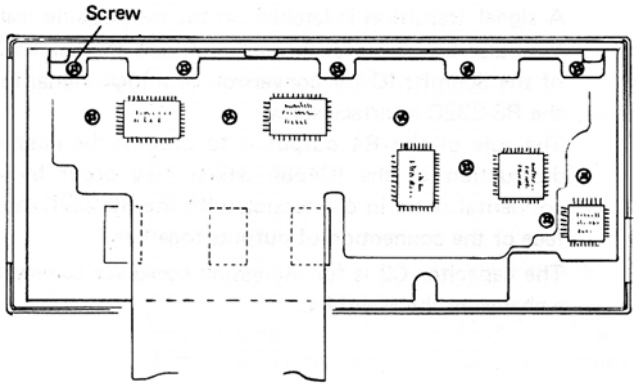
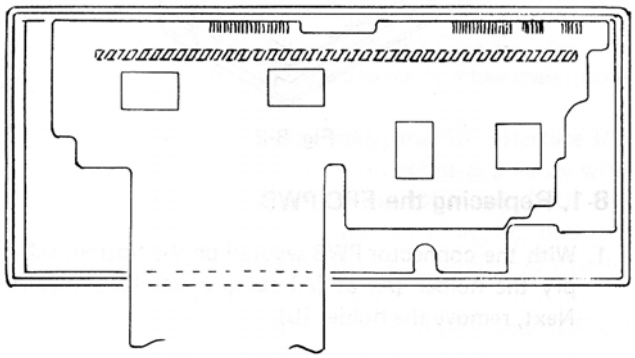


Fig. 8-4

NOTE: Do not drop the rubber connector and rubber spring sheet that are used to hold the soft key. If the electrically conductive part of the rubber connector were to be contaminated, it could be a cause of a failure after the assembly of the unit.

3. Generally, the FPC PWB should not be used again once removed from the key PWB because the soldered pattern might separate from the board.
Since the key PWB is bonded to the FPC PWB, to remove, hold the shadowed portion at (A) with a double tack tape and warm the area with a hair dryer; then separate this portion from the solder using a soldering pencil.



(A)

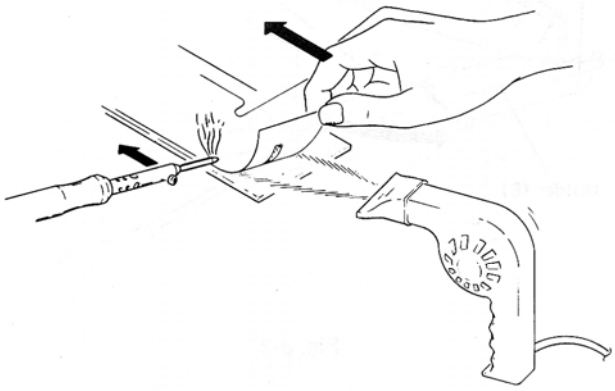


Fig. 8-5

NOTE: This job is required for the reuse of the key PWB.

4. How to solder the FPC PWB with the key PWB
(1) Apply a thin layer of solder over the soldered portion of the FPC PWB.
(2) Cut away 1.5 to 2.0 millimeters of the tip of the FPC PWB using a knife or scissors, in order to check whether the solder melted at the exposed portion Ⓑ of the key PWB will function when heating at (4).
(3) Remove the backing paper of the double tack tape bonded on the back of the FPC and temporarily fit the FPC PWB to the key PWB.
(4) Using a soldering pencil heated to 260° ± 5°C and a pair of tweezers, hold the FPC with the tweezers because the FPC may separate when heated from above. After removing the pencil, hold the FPC with the tweezers for five seconds more.

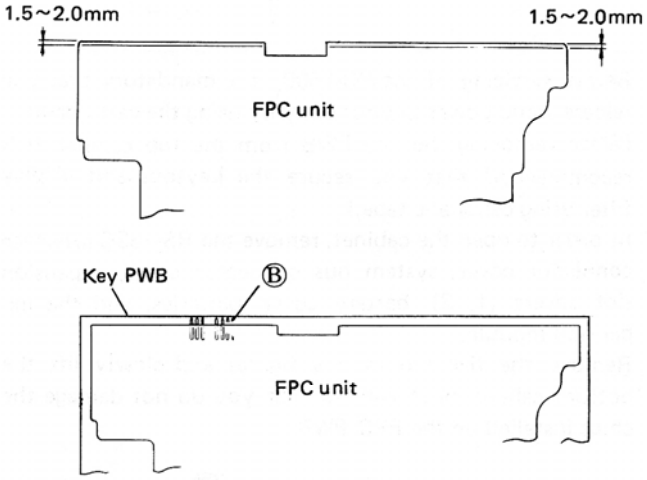


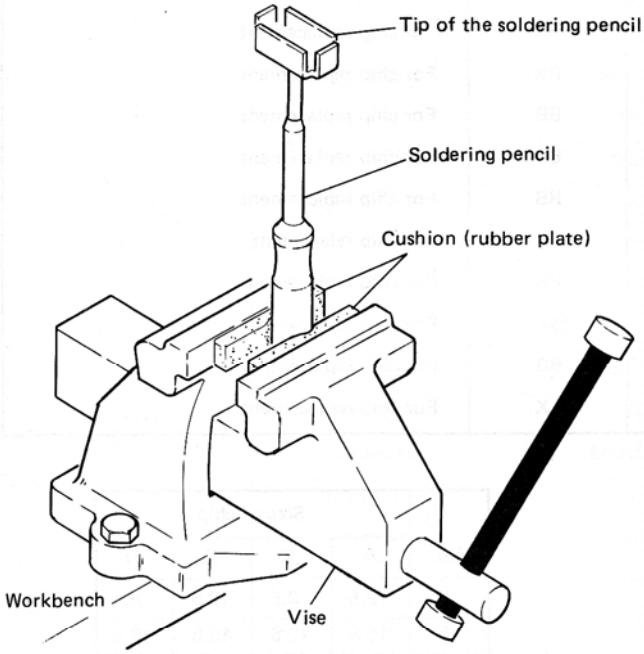
Fig. 8-6

8-2. Removing and installing the LSI and chip components on the FPC PWB

(When a defective component is known without separating the FPC PWB from the key PWB)

(1) Removing the LSI

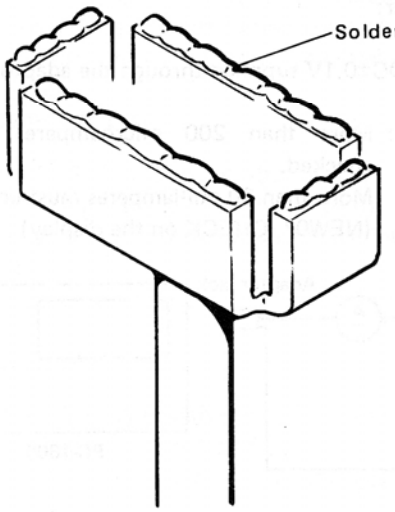
a. Connect the LSI soldering tip to the soldering pencil (see figure), set the surface temperature of the tool to 260°±5°C, and secure it on the vise installed on the workbench.



If it is heated above the given temperature, it might separate the circuit pattern or the FPC PWB itself.

The soldering pencil is held up to prevent solder, flux, and gas from invading the back of the key PWB, where the key contact pattern, the LCD rubber connector, is mounted.

b. Evenly apply a proper amount of flux over the leads of the LSI, and fill up the back side of the chip with solder.



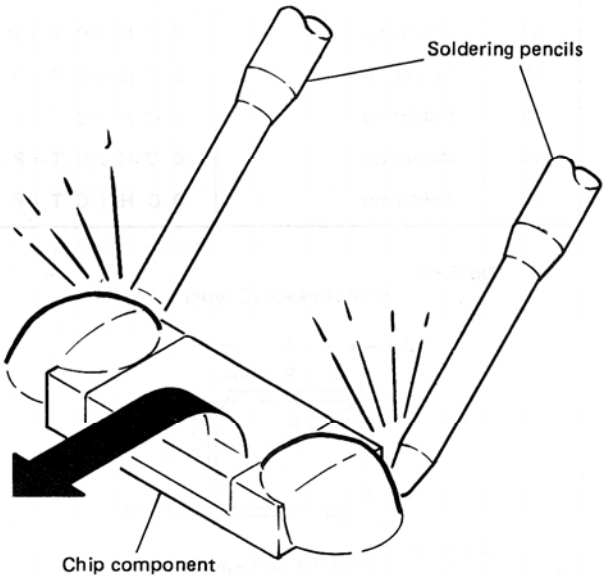
c. Lift the PWB with your hand and carefully mount it over the leads of the LSI. When the solder on the leads melts after five to six seconds, remove the LSI from the PWB using a tweezers (or a small flat tip screwdriver).

d. Clean away solder fragments remaining on the pattern side of the LSI using a solder wick. Then, evenly apply a thin layer of solder over the surface.

e. Apply a small amount of solder to the leads of the new LSI, and solder the leads with care. Press the mold of the LSI with your finger tip while soldering the leads.

(2) How to remove and install the chip component

a. Melt both sides of the chip component using two soldering pencils at the same time. Remove the component quickly.



b. After the removal of the chip component, clean the pattern with a solder wick.

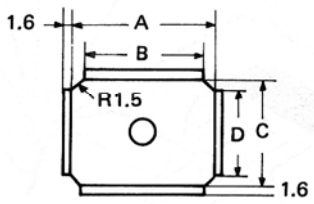
c. Solder one side of the new chip component. Let it cool for ten seconds; then solder the other side.

8-3. List of tools

No.	Parts name	Parts code	Price rank	Use
1	Soldering pencil (FP)	0CH-MACH-FP1V 0CH-MACH-FP2V	BR BS	100~120V 200~240V
2	Solder thermometer	UKOGE0024CSZZ	**	For measurement of solder tip temperature
3	Solder wick	UKOG-0127CSZZ	AT	For absorption of solder
4	Solder tip holder	0CH-FPTiPHOLD	AC	FP solder tip holder
5	Solder tip	0CHiCTiP-1002	BB	For chip replacement
6	Solder tip	0CHiCTiP-1003	BB	For chip replacement
7	Solder tip	0CHiCTiP-1004	BB	For chip replacement
8	Solder tip	0CHiCTiP-1005	BB	For chip replacement
9	Solder tip	0CHiCTiP-1006	BB	For chip replacement
10	Solder tip	0CHiCTiP-1010	BB	For chip replacement
11	Solder tip	0CHiCTiP-1011	BB	For chip relacement
12	Solder tip	0CHiCTiP-1012	BB	For chip replacement
13	Solder tip	0CHiCTiP-1013	BB	For chip replacement
14	Solder tip	0CHiCTiP-1014	BB	For chip replacement
15	Solder tip	0CHiCTiP-1020	AX	For chip replacement

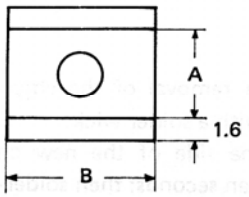
No. 5~9

(Flat package IC type)



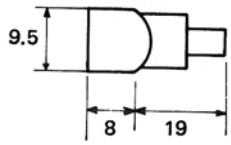
No. 10~14

(Mini-flat package IC type)



No. 15

(Special type)



No.	Size of chip			
	A	B	C	D
5	12.5	9.5	12.5	9.5
6	15.5	12.5	15.5	12.5
7	16.3	13.3	16.3	13.0
8	17.0	14.0	17.0	14.0
9	23.0	20.0	17.0	14.0
10	6.0	5.0	–	–
11	6.0	10.0	–	–
12	7.0	12.5	–	–
13	9.0	15.2	–	–
14	9.0	18.0	–	–

8-4. Measuring power consumption

Supply power:

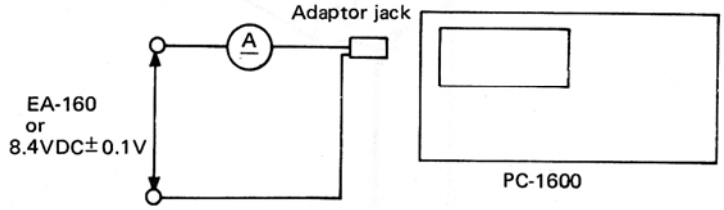
EA-160

Or, 8.4VDC±0.1V supplied through the adaptor jack.

Current:

OFF time: More than 200 microamperes must be checked.

ON time: More than 30 milliamperes must be checked. (NEW0? :CHECK on the display)



Reference

LSI block		SPEC	Actual use	Note
SC7852	IDLE	3.3mA/4MHz	3.3mA/3.58MHz	Dependent on φOS (1.3MHz)
	Operating	30mA/4MHz	26.8mA/3.58MHz	
LH5803	HALT	8mA/3.8MHz	5.5mA/2.6MHz	Not applied at this time.
	Operating	15mA/3.8MHz	10.3mA/2.6MHz	
LU57813P	Standby	50μA	←	For timer only
	Operating	5.0mA/500KHz	3.1mA/307KHz	
LR38041	Standby	10μA	←	
	Operating	10mA/4MHz	3.25mA/1.3MHz	
HD61102	Standby	15μA	←	
	Displaying	100μA	←	
	Accessing	500μA	←	
HD61203		1.0mA/600KHz	0.36mA/217KHz	
TC8576F		10mA/10MHz	1.23mA/1.229MHz	
SC6976T0220	Standby	3μA	←	
	Accessing	15mA/1MHz	6mA/400KHz	
P•ROM	Standby	10μA	←	
	Accessing	8mA/1MHz	3.2mA/400KHz	
RAM	Standby	1.0μA	←	
	Accessing	10mA/1MHz	4.0mA/400KHz	
Power supply (IC regulator IC3)	OFF	100μA	←	
	ON	2.0mA	←	
Power supply (converter IC1)	Display	4.0mA	←	
	SIO operation	28mA	←	
LCD bleeder		0.52mA	←	

Major component consumption power

8-5. Measurement check

The quartz meter must be used in this measurement test.

Tolerance: ±1.5 second/day under ambient temperature of 25°±5°C.

NOTE: Do not perform the measurement test in the early morning as the internal temperature may differ even if the room temperature is within the required limits. The same is applicable to the quartz meter.

8-6. Power-off test

Press the RESET switch on the back of the unit while pressing the ON/BRK key and check for the following:
Power does not turn off within nine minutes (typical is ten minutes).
But, the power turns off within eleven minutes.

8-7. Shock test

With the display digits activated, lift up the display side 45 degrees, then drop it on a desk top.
Then, check to see that there any changes in the display.

8-8. Weak battery detection circuit test

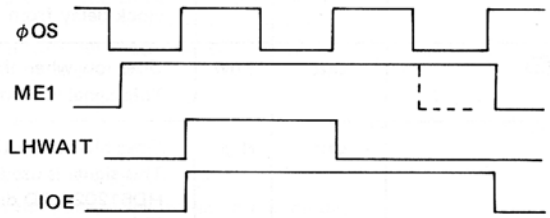
(1) Make sure that the machine operates normally with a supply voltage of 7.0VDC±0.1V.
(2) Make sure that the alarm symbol lights up with a supply voltage of 6.0VDC±0.1V.
(3) Make sure that auto-power-off takes place when the supply voltage is 5.4VDC±0.1V.
(This test must be conducted under the temperature of 25°±5°C or 79.2°±10°F.)

9. LSI pin descriptions

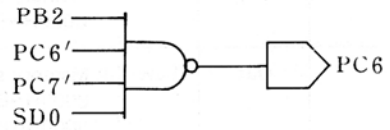
- SC7852 (main CPU 1)
- LH5803 (main CPU 2)
- LU57813P (sub CPU)
- LR38041 (gate array)
- TC8576F (UART)

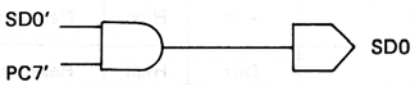
9-1. Main CPU 2 (SC7852) pin description

Pin No.	Symbol	In/Out	Active level	Function
95~ 100~2	$\overline{KIN0}$~$\overline{KIN7}$	▽ In	Low	(1) Internally pulled up to VCC by the resistor (200K ~ 5000K). (2) T input = Low (normal mode) keyboard input. A key in the low input line is pressed. (3) T input = High (emulation mode). Used for connection of the Z-80 ICE.
3	LHWAIT	Out	High	Wait output to the LH-5803. The signal goes high in one of the following: (1) When the WAIT input is at a high level. (2) When the LH-5803 accesses **0*H or 8000H~FFFFH of the ME1 space, it goes high for one cycle time to insert one wait. (3) When the Z-80 is running with the LH-5803 at halt.
4	ϕOS	In	⎍⎍	LH-5803 basic clock (1.3MHz). This clock is used for the sync signal of the internal LH-5810 corresponding port and generation of the LCD CLOCK (217KHz).
5	PT	Out		Memory bank signal.
6	PU	Out		Memory bank signal.
7	PVOUT	Out		Memory bank signal.
8	PVIN	▲ In		LH-5803's PV signal input. As PV is kept in the floating state when the Z-80 is operating, it is internally pulled down by the resistor.
9	$\overline{WR}$	In/Out	Low	(1) When the Z-80 is in operation, the Z-80's $\overline{WR}$ is a direct output on this line. (2) When the LH-5803 is in operation, it becomes an input to enable R/W for the LH-5803.
10~25	A15~A0	▲ In/Out		(1) When the Z-80 is in operation, the Z-80 address bus is an output on this line. (2) When the LH-5803 is in operation, the LH-5803 address bus is an input on this line.
26~33	DB7~DB0	In/Out		Data bus.
34	IORQ	▲ In/Out		(1) When the Z-80 is in operation, the Z-80 $\overline{IORQ}$ is an output on this line. (2) When the LH-5803 is in operation, the LH-5803 ME1 is an input on this line.
35	MREQ	▲ In/Out		(1) When the Z-80 is in operation, the Z-80 $\overline{MREQ}$ is an output on this line. (2) When the LH-5803 is in operation, the LH-5803 ME0 is an input on this line.
36	RD	In/Out		(1) When the Z-80 is in operation, the Z-80 $\overline{RD}$ is an output on this line. (2) When the LH-5803 is in operation, the LH-5803 OD is an input on this line.
37	WAIT	▲ In	High	WAIT input to the Z-80 and LH-5803. Pulled down internally by a resistor.
38	LHA90	Out		Among the RAMs (the bank of the spaces C000H~FFFFH) connected to the RAM3, it is an input to the address A9 of the RAM of E000H~FFFFH (the side A13A is input to $\overline{CE}$1). (1) When the Z-80 is in operation, "LHA90 = A9" is established. (2) Except that "LHA90 = high" is established when the LH-5803 accesses 7400H~744FH and 7500H~754FH. In other words, when the LH-5803 tries to access 7400H~744FH and 7500H~754FH, it actually accesses 7600H~764FH and 7700H~774FH.

Pin No.	Symbol	In/Out	Active level	Function
39	$\overline{M1}$	Out	Low	(1) When the Z-80 is in operation, the Z-80 $\overline{M1}$ is an output on this line. (2) When the LH-5803 is in operation, the signal created from the OPF signal of the LH-5803 is sent on this line.
40	$\overline{RFSH}$	Out	Low	Refresh signal. (1) The Z-80 $\overline{RFSH}$ signal is on this line. (2) When the LH-5803 is in operation, the signal created from the OPF signal of the LH-5803 is sent on this line.
41	VDD			VCC
42	IOE	Out	High	This signal is issued when the LH-5803 tries to access **00H~**0FH and 8000H~0FFFH of the ME1 space. When this signal is sent out, one wait is sent to the LH-5803. In terms of timing, the signal is sent with a half clock delay on the ME1. 
43	$\overline{CS001}$	Out	Low	Z-80 control ROM select signal. 0000H~7FFFH memory space (bank 0).
44	$\overline{CS123}$	▽Out	Low	(1) Z-80 control ROM select signal. 8000H~BFFFH memory space (bank 6). (2) LH-5803 control ROM select signal. C000H~FFFFH memory space.
45	$\overline{CS24}$	Out	Low	Z-80 control ROM select signal. (1) 4000H~7FFFH memory space (bank 3). (2) 8000H~C000H memory space (bank 4). One wait is inserted.
46 47 48	$\overline{LHS3}$ $\overline{LHS2}$ $\overline{LHS1}$	Out ▽ Out ▽ Out	Low Low Low	Memory select signal. Depending on the state of bit "6" of I/O 3CH, the memory space selected differs. $\overline{LHS1}$ and $\overline{LHS2}$ are pulled up internally. $\overline{LHS3}$ needs to be pulled up externally. (pulled up externally.)
49	RAM3	Out	High	Memory select signal (internal 16KB RAM). C000H~FFFFH (bank 0).
50	$\overline{RAM2}$	Out	Low	Memory select signal (S1:). 8000H~BFFFH (bank 0, bank 1). 8000H~BFFFH (bank 2, bank 3).
51	$\overline{RAM1}$	Out	Low	Memory select signal (S2:). 8000H~BFFFH (bank 2, bank 3).
52	SLCT	In	High	When this signal is at low, output of the memory and I/O select signal is disabled. Disabled signals are: $\overline{CS001}$, $\overline{CS123}$, $\overline{CS24}$, RAM3, $\overline{RAM2}$, $\overline{RAM1}$, IOE, $\overline{IOSU}$, $\overline{KA2}$, $\overline{KA1}$, $\overline{KA0}$, C/D, and $\overline{IORP}$. This input is an output to the subcontroller and is at a high level when the system is on.

	b6 = 0	b 6 = 1
$\overline{LHS1}$	A800H~AFFFH (bank 0)	B000H~B7FFH (bank 0)
$\overline{LHS2}$	B000H~B7FFH (bank 0)	A800H~FAFFH (bank 0)
$\overline{LHS3}$	B800H~BFFFH (bank 0)	A000H~A7FFH (bank 0)

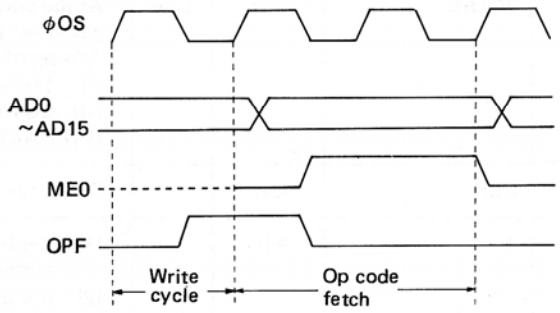
Pin No.	Symbol	In/Out	Active level	Function
53	$\overline{KA2}$	Out	Low	Goes low when the Z-80 I/O 28H~2FH is written.
54	$\overline{KA1}$	Out	Low	Goes low when the Z-80 I/O 28H~2FH is read.
55	$\overline{KA0}$	Out	Low	Goes low when the Z-80 I/O 60H~6FH is accessed.
56	CK0	Out		A 217KHz ϕOS output. This signal is supplied to the HD61203 (S) LCD driver. This signal is issued only when bit "b4" of the Z-80 I/O 37H is at "1". Bit "b4" is at "0" at power-on, but turns to "1" in the power-on routine to activate the LCD.
57	$\overline{IORP}$	Out	Low	Goes low when the Z-80 reads 33H of I/O. This signal is used by the Z-80 to read the return data from the LU57813P.
58	C/$\overline{D}$	Out	High	Goes high when the Z-80 writes 3DH of I/O. Data are latched at a low to high transition of C/$\overline{D}$. When the signal rises with a half clock delay from IORQ, the data bus is stable.
59	$\overline{IOSU}$	Out	Low	Goes low when the Z-80 I/O 20H~27H is accessed. This signal is used for selection of the TC8576F UART.
60	E	Out	High	Goes high when the Z-80 I/O 40H~5FH is accessed. This signal is used to interface with the 6800 series LSI and is connected to the HD61202 LCD driver input. This signal is issued with a half clock delay slower than IORQ.
61	DME0	Out	High	LH-5803 memory select signal. This signal goes high when the LH-5803 accesses the memory.
62~70	PA0~PA7	▽ In/Out		Corresponds to the port PA of the LH-5810 I/O port. This signal is used for the key strobe signal. To restore the original state of the low-forced strobe signal, this signal must be turned high and then set in the input mode. The input signal is pulled up internally.
65	VSS			±0V
71	PB2	▽ In		Used for the cassette tape to reproduce a signal. Pulled up internally.
72	PB5	▽ In/Out		Used for an input port by the PC-1600. Input to this line is a 1/64 second pulse which is issued from the LU57813P sub-controller. Pulled up internally.
73	PB6	▽ In/Out		Used for the key strobe signal. Application is the same as for the PA7~PA0. Pulled up internally.
74	PB7	▲ In		Receives the state of the BREAK/ON key sent from the subcontroller. Pulled down internally.
75	PC6	Out		Used by the Z-80 for a beep generation. The following circuit is internally composed in the LSI.  When either the PB2, PC6', PC7', or SD0 goes low, PC6 becomes high. To drive the buzzer, one of signals issues a pulse.

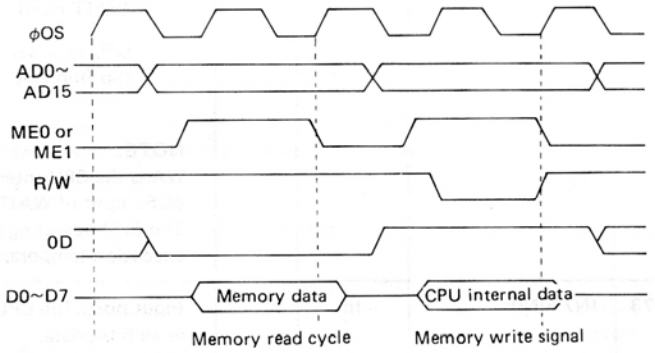
Pin No.	Symbol	In/Out	Active level	Function
				PB2: Cassette reproducing signal. PC6′: Beep disable signal. PC7′: Cassette recording signal (PC-1600). SD0′: Cassette recording signal (PC-1500).
76	SD0	Out		Cassette recording signal output.  SD0′ is the cassette recording output by the CE-150. PC7′ is the cassette recording output by the CE-1600P.
77	$\overline{\text{ELH}}$	Out		(1) A low state of this signal indicates that the LH-5803 is in operation. (2) A high state of this signal indicates that the Z-80 is in operation.
78	PCSTB	In/Out		(1) Goes into the input mode when reset. This current state is latched in the PB3 flip-flop. Therefore, either pulled down or up by an external resistor. For the PC-1600, the machine version is represented by this signal. PB3 = 0: Japan version PB3 = 1: Export version (2) Goes to the output line in the normal mode. The signal goes high when the Z-80 writes 18H or I/O or the LH-5803 is F008H of the ME1. This signal is not used in the output mode with the PC-1600.
79	$\overline{\text{RSTIN}}$	In	Low	A reset input to the SC7852. This signal is forced low for 30 milliseconds by the sub CPU when ACL or RESET is issued or at power-on.
80	IRQ	▲ In	High	An interrupt to the CPU (Z-80, LH-5803). This line is input as an interrupt request from the PC-1500 peripheral.
81	INT0	In	High	An interrupt to the CPU. This line is input as an interrupt request from the T8576F.
82	$\overline{\text{INT1}}$	▽ In	Low	An interrupt to the CPU. This line is input as an interrupt request from the PC-1600 peripheral. Pulled up internally.
83	$\overline{\text{INT4}}$	In	↓	An interrupt to the CPU. An interrupt is sent to the CPU at a high to low transition. This line is input at a 1/64 second pulse from the sub CPU. It is externally shorted with PB5. But, the sub CPU output, which is a P-ch open drain, is pulled down by the external resistor to assure a low output.
84	INT6	▲ In	High	An interrupt to the CPU. This line inputs the output from the sub CPU.
85	PCTRL	Out	Low	At the time the power-off command is sent to the sub CPU, the sub CPU turns the power off (active low). This signal goes low after the Z-80 completes the following: (I) 11H written to I/O 37H (II) OUT (38H), A (III) HALT
86	CLK	Out		Z-80 clock output. 3.58MHz for the PC-1600.
87	T	▲ In		(1) It is in the normal mode when a low signal is received and the Z-80 is operating normally. Pulled down internally. (2) It is in the simulation mode when a high signal is received. The Z-80 bus is in the floating state, and the Z-80 (or Z-80 ICE) can be connected externally.
88 89	XOUT XIN	Out In		The 3.58MHz Z-80 clock is supplied when the oscillator is attached across these lines.
90	VDD			Power input to the high side (4~5.5V).

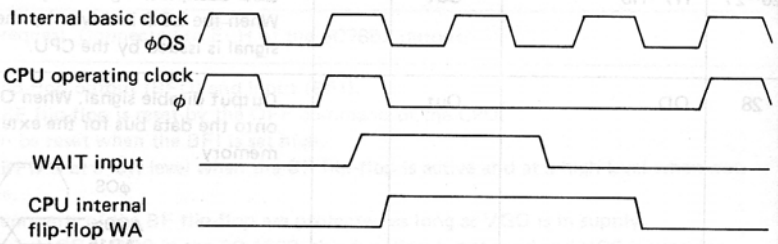
Pin No.	Symbol	In/Out	Active level	Function
91	LHMIO	Out	High	An interrupt is sent to the SC7852. When there is an interrupt request to the LH-5803, this signal goes high.
92	LHNMIO	In/Out	High	(1) Goes high when the LH-5803 is 94**H and when PU = PV is high (CE-158 internal ROM). (2) Becomes an input during reset. So, it must be pulled up or down with the external resistor. With the PC-1600, it is pulled down.
93	LHOPFI	▲ In	High	Receives the OPF output of the LH-5803. Pulled down internally.
94	RSTO	Out	High	Reset output (high) to the LH-5803. When a reset is issued to the Z-80 ($\overline{\text{RSTIN}}$ at low), it makes RSTO high. The rest can only be cleared when the Z-80 first hands down the control to the LH-5803. With this the LH-5803 starts to run.

△: Pulled up to VCC with the internal resistor, 200K ohms ~ 500K ohms.
▲: Internal resistance of 200K ohms ~ 500K ohms is active when the CPU is on, but no MOS resistance is met when the CPU is off.

9-2. Main CPU 1 (LH5803) pin description

Pin No.	Symbol	In/Out	Active level	Function
1	RESET	In		CPU reset input. A high on this line causes the reset. The contents of the address FFFEH are transferred to the PH register and the contents of FFFFH to the PL register. When the reset input changes from high to low, the program starts to execute from the address set in the program counter.
2	(NC)	–		
3	BRQ	In		Bus request. Connected to $\overline{\text{ELH}}$ of the SC7852 output.
4	BFI	In		BF flip-flop output (BFO) and input (BFI). The BF flip-flop is reset by the OFF command of the CPU. It can be reset when the BFI is set high. The BFO is at a low level when the BF flip-flop is active and at a high level when not active. The contents of the BF flip-flop are protected as long as VGG is in supply. Because VGG is VCC in the PC-1600, this function is not used and VCC is used for an input.
5	VGG			Power supply (system's VCC input).
6	BFO	Out		See Pin No.4.
7	OPF	Out		Op code fetch signal which appears when the CPU fetches the OP code. OPF is the signal that is issued only when the operation code is fetched and is not therefore issued in fetching the address data, immediate data, and the second byte of a 2-step command. 
8	BAK	Out		Bus acknowledge signal. When BRQ is set at a high level, the CPU issues a high BAK state in response to it. When BAK is at a high level, the CPU sets the address bus (AD0 ~ AD15), data bus (D0~D7), ME0, ME1, R/W, and OD in high impedance.
9	VCC			Power supply (system's VCC input).

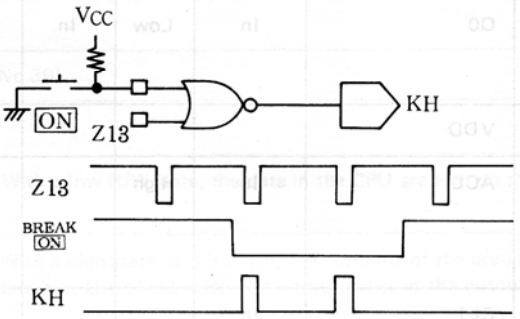
Pin No.	Symbol	In/Out	Active level	Function
10	VGG			Power supply (system's VCC input).
11	VM	In		LCD backplate power supply input.
12	VDis	In		LCD backplate power supply input. Not used by the PC-1600.
13	VA	In		LCD backplate power supply input.
14	VB	In		LCD backplate power supply input.
15	NMI	In		Non-maskable interrupt input. A high input state causes an interrupt to the CPU. The CPU unconditionally accepts the request and starts to execute the interrupt routine from the address whose high order address is represented by the contents of the address FFFCH and the low order address by the contents of FFFDH.
16	MI	In		Maskable interrupt input. When the IE flag (Interrupt Enable) is set on, an interrupt request is caused by a high M1 input state, and the CPU starts to execute the interrupt routine from the address whose high order address is represented by the contents of the address FFF8H and the low order address by the contents of FFF9H.
17	$\overline{\text{HIN}}$	In		Input to the counter by which the LCD and backplate signals, H0~H7, are generated. Normally connected to the HA pin of the CPU. With the PC-1600, this function is not used.
18	HA	Out		CPU internal divider output through which is delivered the basic clock for the LCD driver and connected to $\overline{\text{HIN}}$ and the segment signal generator LSI.
19	DISP	Out		LCD display on/off control signal output. Can be set and reset by means of a command. With the PC-1600, this function is not used.
20~27	H7~H0	Out		LCD backplate signal output. When the LCD is driven by the backplate signal and the segment signal, the backplate signal is issued by the CPU.
28	OD	Out		Output disable signal. When OD is at a high level, the CPU disables the data output onto the data bus for the external device. This signal is issued when writing data in the memory. 
29 30	ME0 ME1	Out Out		Memory enable signal. This signal is enabled to directly access the 128KB memory area; ME0 accesses a 64KB area and ME1 accesses a 64KB area. The memory area accessible by the program counter P and stack pointer S is 64KB, for ME0 is used by the fetch and stack commands. For accessing data, both ME0 and ME1 memory areas can be accessed by the CPU command.
31~38	D0~D7	In/Out		Bidirectional data bus which is used to write data in the external memory or to read data from the external memory.
39~46	A0~A7	Out		Address bus which may be in three states. Goes to high impedance with the BRQ (bus request) signal. It is possible to access the memory area of 64KB. It is also possible to access the memory of 128KB using the ME0 or ME1 signal.

47	GND			Power supply.
48	A8	Out		Address bus (see Pin No.39).
49	VGG			Power supply.
50~56	A9~A15	Out		Address bus (see Pin No.39).
57	(NC)	—		
58	R/W	Out		Memory write signal. With a low R/W state, the data in the CPU are sent on the data bus.
59	Pφ	Out		External latch clock. With a high state of this clock, the contents of the accumulator are transferred onto the data bus. Use of the latch IC permits its use as the output port (see the ATP command).
60 61	PV PU	Out Out		These are the CPU internal flip-flop output pins (PU, PV). There are commands to set and reset PU and PV.
62	φOS	Out		The clock, in the same phase as the CPU internal basic clock, is on this line to supply clock pulse to the external system. When a 2.6MHz crystal is connected across XL0 and XL1, a 1.3MHz clock is supplied.
63 64	XL0 XL1	In Out		Crystal connection pins. XL0 is an input and XL1 is an output. Inside the CPU, the clock is divided in half. When a 2.6MHz crystal is connected, the machine cycle within the CPU is at 1.3MHz.
65	WAIT	In		CPU wait signal. When this input is high, the CPU's internal operation clock "φ" stops and the CPU therefore stops executing a command. When it resumes a low state, the CPU starts to execute a command.  NOTE: WA is the CPU internal flip-flop for WAIT. At a high to low transition of the clock φOS, input of WAIT is accepted. The CPU operating clock φ stops when WA is at high; the CPU halts a command execution temporarily as a result.
66~73	IN7~IN0	In		Input port. The CPU can send the signal input on the IN0~IN7 to the CPU accumulator as an 8-bit data. It has an internal pull-up resistor. When not connected, the CPU assumes the line to be in high impedance.
74~76	(NC)	—		

NOTE: NC: No Connection

9-3. Sub CPU (LU57813P) pin description

Pin No.	Symbol	In/Out	Active level	State at ACL	Function
1	Q0	In	Low	In	When the system-off command is received from the Z-80, the system is turned off after this signal goes low. It has PCTRL output from the SC7852 as its input.
2	VDD				High side VGG is supplied.
3	ACL	In	High		The pulse width of ACL must be greater than 1 microsecond in duration to be recognized by the hardware. It takes about 80 microseconds before the LSI starts to operate after input of ACL. This pin is used as reset input from the ALL RESET switch of the PC-1600.
4 5	CL1 CL2	In Out			The system clock generating ceramic oscillator is attached across these two lines. With the PC-1600, a 1.229MHz oscillator is used for the basic clock of the RS-232C baud rate.
6	FOUT	Out			System clock output. Not used.
7	P0	Out	Low	In	Reset input to the SC7852. This line is maintained low for 30 milliseconds during system-on and reset.
8	P1	Out	Low	In	In a low state when the main CPU is permitted to access the memory and I/O.
9	P2	Out	High	In	In an opposite level of P1. Input to SLCT of the SC7852.
10	P3	Out	Low	In	In a low state during system-on. Used to turn on the system.
11	KH	In	High		This signal goes high with an input of the ON key. When the system is off, this LSI is in the standby mode, and it turns on the system with a high KH state.
12	KI	In	High		A command request from the main CPU. Interrupt is caused by a high K1 state.
13	T	In			Test pin which is NC.
14 15	OSCOUT OSCIN	Out In			The 32.768 KHz timer crystal oscillator is attached across these lines.
16	KL	In	High		Reset input from the peripheral unit. As monitored by the software, if this input is high for more than the given.time, the reset is executed.
17	Z15	Out	High	In	Z15 and KL are shorted outside and externally pulled down by the resistor. Z15 is turned high for 1 millisecond in the reset routine to be converted into the RSTE signal, and sent to peripherals as the reset signal via the system bus. So, both Z15 and KL can be handled as an input/output line, which may be used to apply reset to the peripheral or to receive reset from the peripheral. This signal is used as the reset input of the CE-1600P.
18	Z14	Out	High	In	The sub CPU monitors the state of the BREAK/ON key via the KH input line and its state is sent through Z14 and supplied to PB7 of the SC7852. Therefore, key chattering and bouncing of the BREAK/ON key are completely controlled the sub CPU.
19	Z13	Out	Low	In	The sub CPU goes into the power-down mode except when one of the conditions mentioned below holds true. (1) When a command is received from the main CPU. (2) When a timer interrupt is received. (3) If the BREAK/ON key sensing KH input is at a high level. To prevent these conditions from occurring, Z13 is set low at every time interrupt (1/128 second). If KH is at a high level, depression of the BREAK/ON key is sensed.

Pin No.	Symbol	In/Out	Active level	State at ACL	Function
					
20	Z12	Out	Low	In	For the PC-1600, a high signal state is normally issued (at ON).
21	Z11	In		In	NC.
22	Z10	Out	High	In	This signal is used to interface with the main CPU. it goes high when the sub CPU waits for a command (ready), and goes low when busy.
23	Z9	Out	High	In	This signal is also used to interface with the main CPU. A high pulse is issued when the sub CPU terminates a command execution.
24	Z8	Out		In	Used to setup the analog input mode. (1) Voltage is A/D converted when low (initial value). The input impedance is 100K ohms. (2) Current is A/D converted when high. The PC-1600 supports (1) in BASIC, but it needs to program in machine language for (2).
25	Z7	Out	High	In	The sub CPU sets this signal high when the command specified interrupt has been acknowledged. This signal is connected to INT6 input of the SC7852. There are four causes which force this signal level to high. (I) The weke-up time matched the real-time timer. (II) The time of alarm-1 or -2 matched the real-time timer. (III) Receipt of an input from the external keyboard. (IV) At 0.5 second cycle of the real-time timer. This signal goes low when the interrupt cause status is read or when all inputs from the external keyboard have been read.
26	GND				±0V
27	Z6	Out	Low	In	A 1/64 second pulse of 50% duty is sent. Connected to $\overline{\text{INT4}}$ and PB5 inputs of the SC7852.
28	Z5	Out	High	In	As the reference voltage is required when the sub CPU A/D converts the signal input to KC0~KC2, Z5 is set high only during the A/D conversion to obtain the correct VRH. This is used for VRH accuracy as well as power saving.
29	Z4	Out	High	In	Used for handshaking of the external keyboard input through the analog input connector. Shorted with the analog input KC1. Normally an open output.
30	Z3	In		In	Not used.
31	Z2	In		In	
32	Z1	In		In	
33	Z0	In		In	
34	SOUT	Out			
35	SCLOCK	In/Out		In	
36	F	Out			Used for generation of click and alarm sounds.
37	VRH	In			A/D conversion high side reference voltage (2.475V in supply).

Pin No.	Symbol	In/Out	Active level	State at ACL	Function
38	KC3	In			Not used.
39	KC2	In			Used for checking the CE-1600P power supply level. VPP supplied from the CE-1600P via the system bus is A/D converted. If it is below the given level, the peripheral is assumed to have a weak battery condition.
40	KC1	In			Used for checking the PC-1600 main power supply level. The level of the main power supply is A/D converted and checked. If it is below the given level, a weak battery condition is assumed.
41	KC0	In			Receives the signal input from the analog input connector. (1) For the analog input, A/D conversion is done. (2) For the external keyboard input, its logic level is interrogated.
42	R33	Out		In	MSB Return data to the Z-80. LSB
43	R32	Out		In	
44	R31	Out		In	
45	R30	Out		In	
46	R23	Out		In	
47	R22	Out		In	
48	R21	Out		In	
49	R20	Out		In	
50	VRL				NC
51	SIN	In			NC
52	VDD				High power supply voltage level (VGG).
53	R13	In		In	MSB Command from the Z-80. LSB
54	R12	In		In	
55	R11	In		In	
56	R10	In		In	
57	R03	In		In	
58	R02	In		In	
59	R01	In		In	
60	R00	In		In	
61	Q3	In	Low	In	Hardware sensed weak battery detection signal. A high on this line causes the CPU to force the system to go down. The only means to turn the system on after recovery of power supply is the depression of the BREAK/ON key or ALL RESET switch. The time in the real-time timer would not be revised.
62	Q2	In		In	Not used. Pulled down.
63	Q1	In	Low	In	Opposite polarity as CI of the RS-232C interface. It is possible with CI to turn on the system when the system is off (when this line is at a low level).
64	Q0	In	Low	In	If this signal is at a low level when the system-off command is received from the Z-80, the system is turned off.

9-4. Gate array (LR38041) pin description

This gate array is an integration of ICs required for connection of LSIs.

Pin No.	Symbol	In/Out	Active level	Function
1	SLCB	In		It is an input of the sub CPU-issued signal PI which indicates commencement of the system operation. PI (SLCB) goes high when the system is off and does the following. (1) Data buses, D2~D0, are fixed at a low level. (2) Except for A13A, all output levels are fixed to low or high.
2	Q3	In		Hardware weak battery detect signal. (1) When a weak battery condition is detected, it forces Q3 high; S1, S2, S3, K0, K1, and K2 outputs are set high; KH output is set low; and RD is set to high impedance (inactive). (2) Q3 is at a low level when a weak battery is not established.
3	Z12	In		When on, the input is high.
4	Z13	In	Low	The sub CPU is normally in the sandby mode to save power when a command is not received. But, it would not go into the power save mode if the BREAK/ON key is continuously depressed, as it goes out of the standby mode if KH is at a high level. To prevent this, the state of the BREAK/ON key must be interrogated with Z13 when required. During the power save mode, Z13 is set to high to keep the KH output at a low level.
5	ON	In	Low	BREAK/ON key input. The signal goes low when the BREAK/ON key is depressed; otherwise, it is in a high state.
6	KC1	In		Signal input from the analog input connector.
7	CL2	In		Sub CPU 1.229MHz clock input.
8	RD	Out	Low	Read signal created by five signals (ME0, ME1, OD, CK0S, and BR0) which are externally wired OR with RD of the Z-80. When the Z-80 is in operation, RD is at a high impedance.
9~16	R20~R33	In		Return data from the sub CPU. The data becomes the Z-80 data when the Z-80 reads 33H of I/O.
17	PRIM	In		The PC-1600 has two serial input/output interface: the RS-232C interface and the SIO interface. But, either one must be assigned as only one hardware is for the serial input/output. (1) The SIO interface is selected with a low PRIM state. (2) The RS-232C interface is selected with a high PRIM state.
18	TXD	In	Low	Transmit data which is an output from the T8576F UART.
19	RXD	Out	Low	Receive data which is an input to the T8576F UART.
20	RDA	In	Low	Receive data which is an input from the RS-232C interface.
21	SDA	Out	High	Transmit data output is sent through the RS-232C interface connector. A low signal state is sent when PRIM is at a low level.
22	RDF	In	High	Receive data which is an input from the SIO interface.
23	SDF	Out	High	Transmit data which is an output to the SIO interface connector. A low signal state is sent when PRIM is at a high level.

	PRIME = "Low"	PRIME = "High"
Output SDA	LOW	$\overline{\text{TXD}}$
Output SDF	$\overline{\text{TXD}}$	LOW
Input RXD	RDF	RDA

Pin No.	Symbol	In/Out	Active level	Function
24	CKOS	In		The OD signal indicates that the CPU (LH5803) read timing is at a low level when not writing, So, it may possibly be at a low level when not reading, and it also may not match the Z-80's timing during data input/output of the SC7852 internal data. To prevent these problems, the signal goes low only when the LH-5803 is reading the memory or I/O is created with five signal (ME0, ME1, OD, CK0S, and BR05).
25	VCC	—		Power supply (input of VGG of the system).
26	GND	—		Power supply.
27	BRQ	In		See Pin No. 24.
28~30 31~35	D0~D2 D3~D7	In/Out Out		Z-80 data bus. When the sub CPU output P1 (SLCB), which is sent out when the system is off, is at a high level, D2~D0 become low, thus fixing the level of the input sinal during system-off as D2~D0 are inputs also.
36	C/$\overline{D}$	In	High	The C/$\overline{D}$ line of the SC7852 goes high when the Z-80 wirites 3DH of the I/O.
37	$\overline{IORP}$	In	Low	The signal used to send R33~R20 on the Z-80 data bus. It goes low when the Z-80 reads 33H of the I/O.
38	$\overline{CL}$	In	Low	System reset input. When this signal is at a low level, it forces A16A to high, A15A to low, and A14A to high.
39	A13	In		CPU address A13.
40	A14	In		Input of the CPU address A14 (insignificant).
41	DSR	Out		Not used.
42	CLK1	Out		When the system is on, CL2 is issued on this line and becomes the basic clock for the UART. A low is on this line when the system is off.
43	KH	Out	High	Opposite polarity of the BREAK/ON key input is sent to the sub CPU.
44	A13A	Out		Opposite polarity of the A13 input is sent.
45~47	A14A~A16A	Out		C/D latched D2~D0 output. Also, A16A is used for separating the $\overline{CS24}$ selected 16KB memory space 4000H~7FFFH (bank 3) into two banks.
48~50 51~53	LHS1~LHS3 KA0~K2	In In	Low Low	Memory select and I/O select signals from the SC7852 are sent to slots of S1: and S2: via the gate array. The reason why is that it has to be set at a high level at system-off as the SC7852 power supply is shut off when the system is off. (1) When the system is on but not in a weak battery condition the status of each signal appears on S1, S2, S3, KD, K1, and K2. (2) All are high when the system is off or a weak battery is detected.
54~56 59~61	S1~S3 K0~K2	Out Out	Low Low	LHS1~KA2 outputs. All are high outputs when the system is off.
62 63 64	ME1 ME0 OD	In In In		See pin No.24.

9-5. TC8576F UART pin description

The TC8578P Standard Microcomputer Interface (SMI) is a single chip C-MOS LSI which supports the RS-232C serial interface and Centronics compatible parallel interface, both of which are standard interfaces for microcomputers.

In the LSI is contained the RS-232C ART (Asynchronous Receiver Transmitter), its baud rate generator, and the Centronics transmitter/receiver interface. For the Centronics interface, either the transmitter or the receiver mode must be selected.

When the ART receives data from the CPU, the data are converted into serial form and sent out on the TXD line. On the other hand, the serial data received on the RCD line are converted into parallel form before being handed to the CPU. The ART is able to inform the CPU at any time of the completion of sending the data received from the CPU or the reception of the data to be handed to the CPU.

The clock input of the IC is divided by a 4-bit programmable prescaler and becomes the internal clock (SYS-CLK), which is further divided by the baud rate generator composed of a 12-bit programmable divider, for the creation of any baud rate of 50 to 38,400 bauds.

The transmission/reception handshake pins are provided for the Centronics parallel interface. When the 8-bit data are received from the CPU in the transmit mode, a strobe of the programmed pulse width is automatically issued. In the receive mode, when data are received with a strobe singal from the external source, a busy singal is returned to automatically inform the CPU.

Pin No.	Symbol	In/Out	Active level	Function
1	(NC)	—	—	Not used.
2	$\overline{RD}$	In	Low	A low on this line causes the CPU to read data or status information from the SMI.
3	$\overline{WR}$	In	Low	A low on this line causes the SMI to receive data or control words sent from the CPU via the data bus.
4	$\overline{CS}$	In	Low	A low on this line causes the SMI to be activated. When $\overline{CS}$ is at a high level, both $\overline{RD}$ and $\overline{WR}$ are disabled.
5, 6	A1, A0	In	—	In combining this signal with $\overline{RD}$ or $\overline{WR}$, the CPU selects the contents of the data transfer with the SMI.
7	GND	Power supply	—	Power supply.
8	INT	Out	High	Logical OR of four internal signals (RXRDY, TXRDY, PRRDY, and PTRDY) which is used to cause an interrupt to the CPU.
9~16	D7~D0	In/Out	—	Data bus.
17	VCC	Power supply	—	Power supply.
18	GND	Power supply	—	Power supply.

A1	A0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	Function
0	0	0	1	0	RXD → data bus, serial
0	0	1	0	0	Data bus → TXD, serial
0	1	0	1	0	PIN → data bus, parallel
0	1	1	0	0	Data bus → PVOUT, parallel
1	0	0	1	0	Serial status → data bus
1	0	1	0	0	Data bus → parameter register
1	1	0	1	0	Parallel status → data bus
1	1	1	0	0	Data bus → command + parameter address
*	*	*	*	1	Data bus, high impedance
*	*	1	1	0	Data bus, high impedance

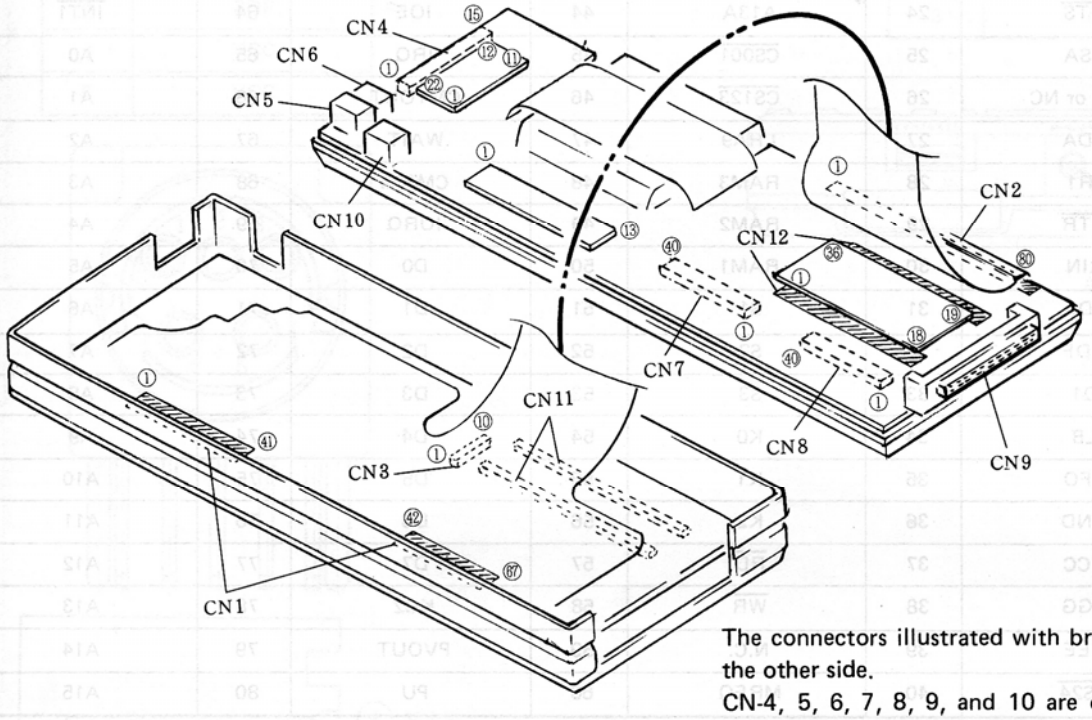
* don't care

Pin No.	Symbol	In/Out	Active level	Function
19~26	$\overline{DATA1}$~$\overline{DATA8}$	In/Out	—	Bidirectional parallel data bus fixed to the output mode. The input mode is established with a high CDS state and the output mode is established with a low CDS state. The contents of data are in the reverse phase.
27	DSTB	In/Out	—	Parallel mode data strobe signal. Data strobe is sent when CDS is "1." Data strobe is received when CDS is "0."
28	ACK	In/Out	—	Parallel mode acknowledge signal. ACK is sent when CDS is "1." ACK is received when CDS is "0."
29	FAULT	In/Out	—	Parallel mode fault signal. When CDS is "1," the contents of the bit "0" of the command byte are sent out. When CDS is "0," the contents of this signal line can be known by the status bit "0." Mainly used for detection of a fault in the device.
30	$\overline{BUSY}$	In/Out	—	Parallel mode busy signal. When CDS is "1," a busy signal is sent. When CDS is "0," a busy signal is received.
31	PRIME	In/Out	—	Parallel mode input PRIME signal. When CDS is "1," it serves as a single bit input port. When CDS is "0," it serves as a single bit output line, but it still would be possible to choose a high level, low level, or one-shot pulse signal.
32	$\overline{SLCT}$	In/Out	—	Parallel mode select signal. When CDS is "1," the contents of the bit "1" of the command byte are sent out. When CDS is "0," the contents of this signal line can be known by the status bit "1." Mainly used for a device select.
33	$\overline{RTS}$	Out		Serial mode request to send signal. A general purpose 1-bit output port in the reverse phase. By programming the bit "5" of the command byte, it is set to "0." The signal is normally used by the modem control as a request to send.
34	$\overline{DSR}$	In		Serial mode data set ready signal. A general purpose 1-bit input port in the reverse phase. It is possible to know the state of the signal by interrogating the status information (bit 7) of the serial interface. This signal is normally used for tests by the modem for such as a data set ready. With the PC-1600, this signal is connected with the RXD line.
35	$\overline{CTS}$	In		Serial mode clear to send signal. Connected to GND. If the TXEN bit of the command byte has been set to "1," a high on this line enables the SMI transmit (serial).
36	$\overline{DTR}$	Out	—	Serial mode data terminal ready signal. A general purpose 1-bit input port in the reverse phase. By programming the bit "5" of the command byte, it is set to "0." The signal is normally used for the modem control as a data terminal ready.
37	TXD	Out	-	Serial mode transmit data signal. Serial data output for the serial interface.
38	RXD	In	—	Serial mode receive data signal. Serial data input for the serial interface.
39	VCC	Power supply	—	Power supply.
40	CDS	In	—	Parallel mode direction selection line. Fixed to GND, it's an input signal to determine the direction of the parallel interface. When the signal is at a low level, the parallel interface is operated in the output mode. When the signal is at a high level, the parallel interface is operated in the input mode.
41	XCLK	In	—	Fixed to GND. This line is an input to the internal 4-bit programmable prescaler. Its output becomes the system clock (SYS-CLK) which is used for internal timing generation and baud rate generation. Normally, 400KHz~10MHz is used as the system clock frequency.

Pin No.	Symbol	In/Out	Active level	Function
42	$\overline{\text{RESET}}$	In	Low	IC reset pin. A low on this line disables all the functions of the IC.
43	P5V	In/Out	—	Parallel mode signal which is fixed to GND. When CDS is "1," it serves as a 1-bit output port. When CDS is "0," it serves as a supply voltage input of the external device.
44	$\overline{\text{PE}}$	In/Out	—	Parallel mode paper end signal. When CDS is "1," it serves as a 1-bit output port. When CDS is "0," it receives the paper end signal from the external device.

10. Connection locations and interface signal identification

Shown below is the breakdown view of the system after removeing the five screws. Connector numbers are indicated.



The connectors illustrated with broken lines are located on the other side.
CN-4, 5, 6, 7, 8, 9, and 10 are connected with the connector.
CN-1 and 2 are connected with solder.
CN-2, 3, and 11 are pressure fitted using rubber connectors and springs.

List of connector numbers

CN-1 (FPC PWB and key PWB)

Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name
1	VCC	18	D0	35	PA2	52	CDA
2	GND	19	D1	36	PA1	53	P5V
3	KIN0	20	$\overline{RD}$	37	PA0	54	$\overline{DTR}$
4	KIN1	21	D2	38	E	55	$\overline{DATA8}$
5	KIN2	22	D3	39	IOSU	56	$\overline{DATA7}$
6	KIN3	23	D4	40	CK0	57	$\overline{DATA6}$
7	KIN4	24	D5	41	RSTIN	58	$\overline{DATA5}$
8	KIN5	25	D6	42	VGG	59	$\overline{DATA4}$
9	KIN6	26	D7	43	RXD	60	$\overline{DATA3}$
10	KIN7	27	INT0	44	TXD	61	$\overline{DATA2}$
11	$\overline{WR}$	28	PC6	45	PR1	62	$\overline{DATA1}$
12	A5	29	PB6	46	$\overline{DSR}$ or NC	63	VEE
13	A4	30	PA7	47	XCLK	64	DSTB
14	A3	31	PA6	48	ON	65	$\overline{BUSY}$
15	A2	32	PA5	49	$\overline{RTS}$	66	ACK
16	A1	33	PA4	50	CSA	67	F
17	A0	34	PA3	51	DRA		

CN-2 (FPC PWB and connector PWB)

Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name
1	ACL	21	A16A	41	φOS	61	P.T
2	SDA	22	A15A	42	DME0	62	RSTE
3	RDA	23	A14A	43	$\overline{\text{ELH}}$	63	$\overline{\text{M1}}$
4	$\overline{\text{RTS}}$	24	A13A	44	IOE	64	$\overline{\text{INT1}}$
5	CSA	25	$\overline{\text{CS001}}$	45	IRQ	65	A0
6	DRA or NC	26	$\overline{\text{CS123}}$	46	CMTOUT	66	A1
7	CDA	27	LHA9	47	WAIT	67	A2
8	PR1	28	RAM3	48	CMTIN	68	A3
9	$\overline{\text{DTR}}$	29	RAM2	49	IORQ	69	A4
10	AIN	30	RAM1	50	D0	70	A5
11	SDF	31	S1	51	D1	71	A6
12	RDF	32	S2	52	D2	72	A7
13	Q1	33	S3	53	D3	73	A8
14	LB	34	K0	54	D4	74	A9
15	BFO	35	K1	55	D5	75	A10
16	GND	36	K2	56	D6	76	A11
17	VCC	37	$\overline{\text{RD}}$	57	D7	77	A12
18	VGG	38	$\overline{\text{WR}}$	58	KC2	78	A13
19	VEE	39	N.C.	59	PVOUT	79	A14
20	$\overline{\text{CS24}}$	40	MREQ	60	PU	80	A15

CN-3 (key PWB and programmable function key)

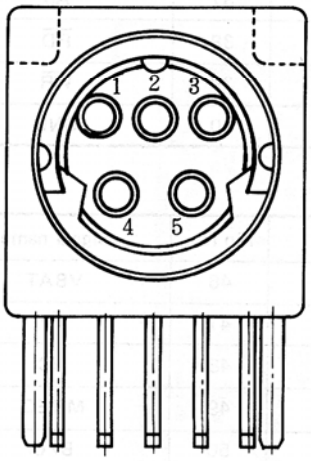
Pin No.	Signal name
1	PA6
2	KIN4
3	KIN1
4	PA1
5	PA4
6	PA5
7	PA7
8	PA2
9	PA3
10	PB6

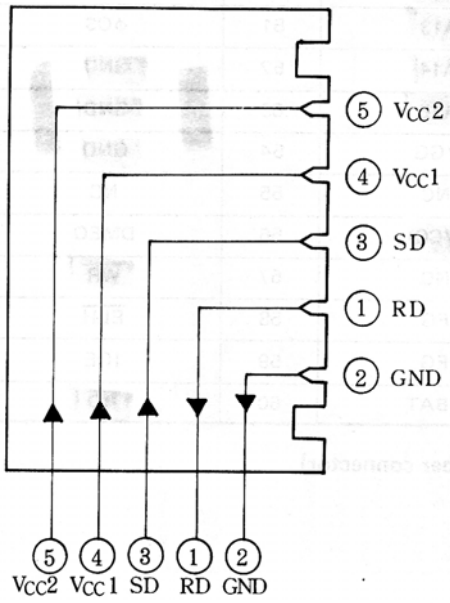
CN-4 (RS-232C connector)

Pin NO.	Signal name
1	FG
2	SD (TXD)
3	RD (RXD)
4	RS (RTS)
5	CS (CTS)
6	DS (DSR)
7	SG (GND)
8	CD
9	CI
10	VC1
11	NC
12	NC
13	NC
14	ER (DTR)
15	NC

CN-5
(SIO (FIVER) connector)

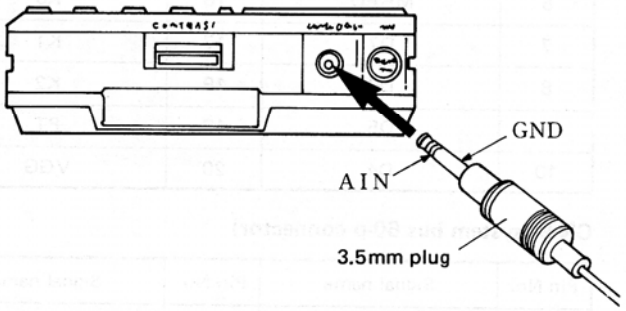
Pin No.	Signal name
1	RDF
2	GND
3	SDF
4	VCC
5	VCC





CN-6
(analog input connector)

Pin No.	Signal name
1	GND
2	Not used.
3	AIN



CN-7 (S1: slot 1 connector)

Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name
1	VCC	11	D3	21	NC	31	A6
2	PVIN	12	D2	22	A15	32	A5
3	PU	13	D1	23	A14	33	A4
4	RAM2	14	D0	24	A13	34	A3
5	PVOUT	15	INH	25	A12	35	A2
6	MREQ	16	S1	26	A11	36	A1
7	D7	17	S2	27	A10	37	A0
8	D6	18	S3	28	A9	38	$\overline{RD}$
9	D5	19	PT	29	A8	39	$\overline{WR}$
10	D4	20	VGG	30	A7	40	GND

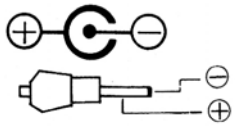
CN-8 (S2: slot 2 connector)

Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name
1	VCC	11	D3	21	NC	31	A6
2	PVIN	12	D2	22	A15	32	A5
3	PU	13	D1	23	A14	33	A4
4	RAM1	14	D0	24	A13	34	A3
5	PVOUT	15	INH	25	A12	35	A2
6	MREQ	16	K0	26	A11	36	A1
7	D7	17	K1	27	A10	37	A0
8	D6	18	K2	28	A9	38	$\overline{RD}$
9	D5	19	PT	29	A8	39	$\overline{WR}$
10	D4	20	VGG	30	A7	40	GND

CN-9 (system bus 60-p connector)

Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name
1	A7	16	PVOUT	31	A8	46	VBAT
2	A6	17	D7	32	A9	47	VP
3	A5	18	D6	33	A10	48	NC
4	A4	19	D5	34	A11	49	MREQ
5	A3	20	D4	35	A12	50	BFO
6	A2	21	D3	36	A13	51	ϕOS
7	A1	22	D2	37	A14	52	GND
8	A0	23	D1	38	A15	53	GND
9	$\overline{INT1}$	24	D0	39	VGG	54	GND
10	$\overline{M1}$	25	INH	40	NC	55	NC
11	VCC	26	IORQ	41	VCC	56	DMEO
12	NC	27	CMTIN	42	NC	57	$\overline{WR}$
13	RSTE	28	WAIT	43	FG	58	$\overline{ELH}$
14	PT	29	CMTOUT	44	FG	59	IOE
15	PU	30	IRQ	45	VBAT	60	$\overline{RD}$

CN-10 (AC adaptor)



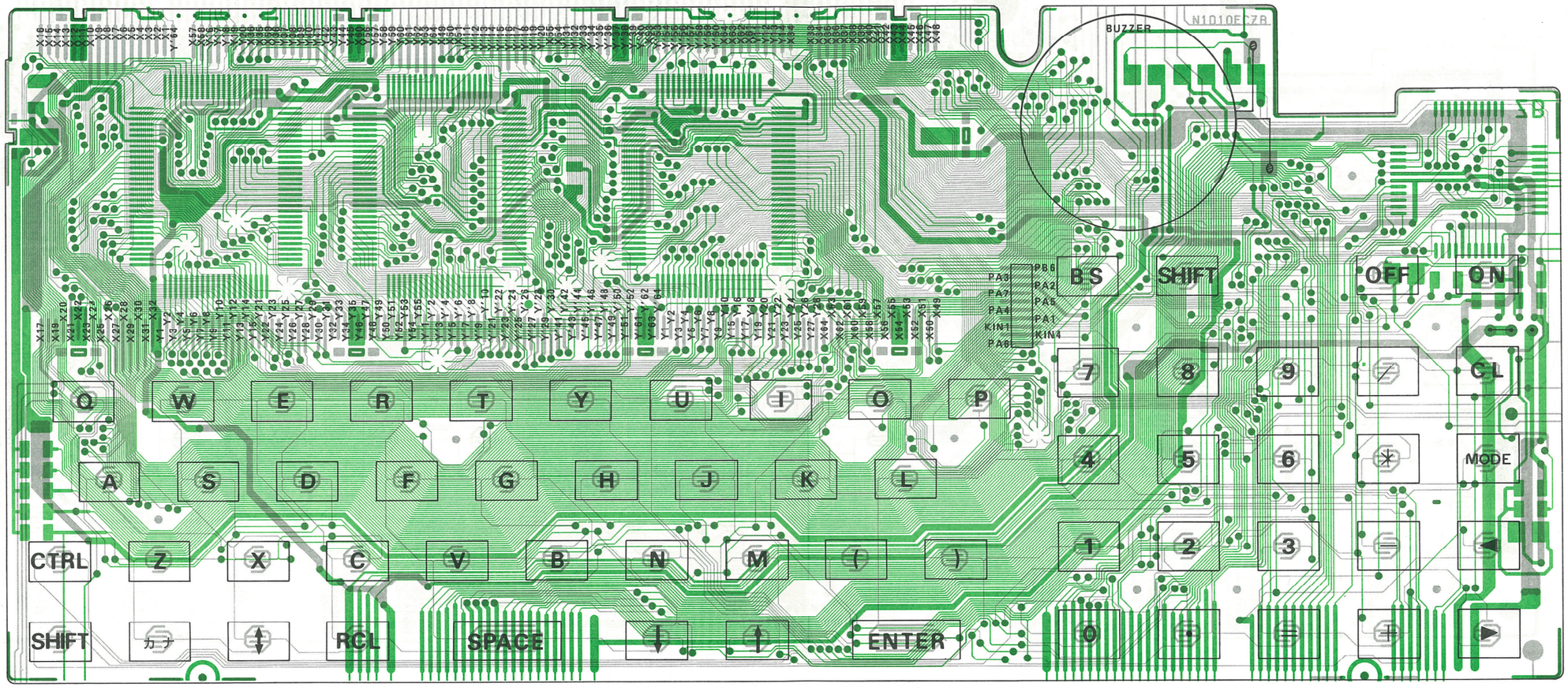
CN-11 (LCD rubber connector)

CN-12 (PWB memory and PWB connector)

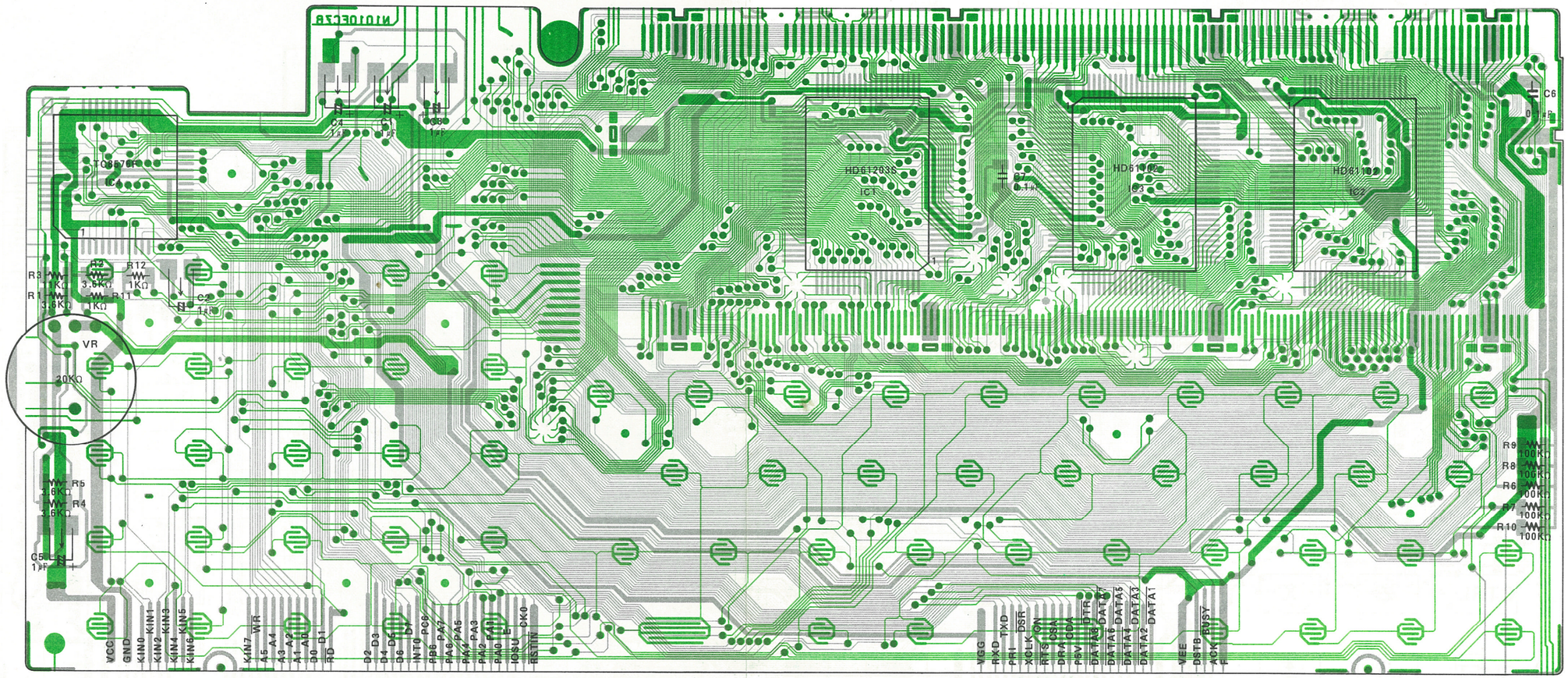
Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name	Pin No.	Signal name
1	VGG	10	A10	19	GND	28	A4
2	$\overline{WR}$	11	A13	20	$\overline{CS001}$	29	A5
3	RAM3	12	D7	21	D2	30	A6
4	A8	13	D6	22	D1	31	A7
5	A9	14	D5	23	D0	32	A12
6	LHA90	15	D4	24	A0	33	$\overline{CS123}$
7	A11	16	D3	25	A1	34	A14
8	A13A	17	INH	26	A2	35	A15
9	$\overline{RD}$	18	VCC	27	A3	36	$\overline{CS24}$

11. CIRCUIT DIAGRAM · PARTS POSITION

KEY P.W.B. (LCD SIDE)



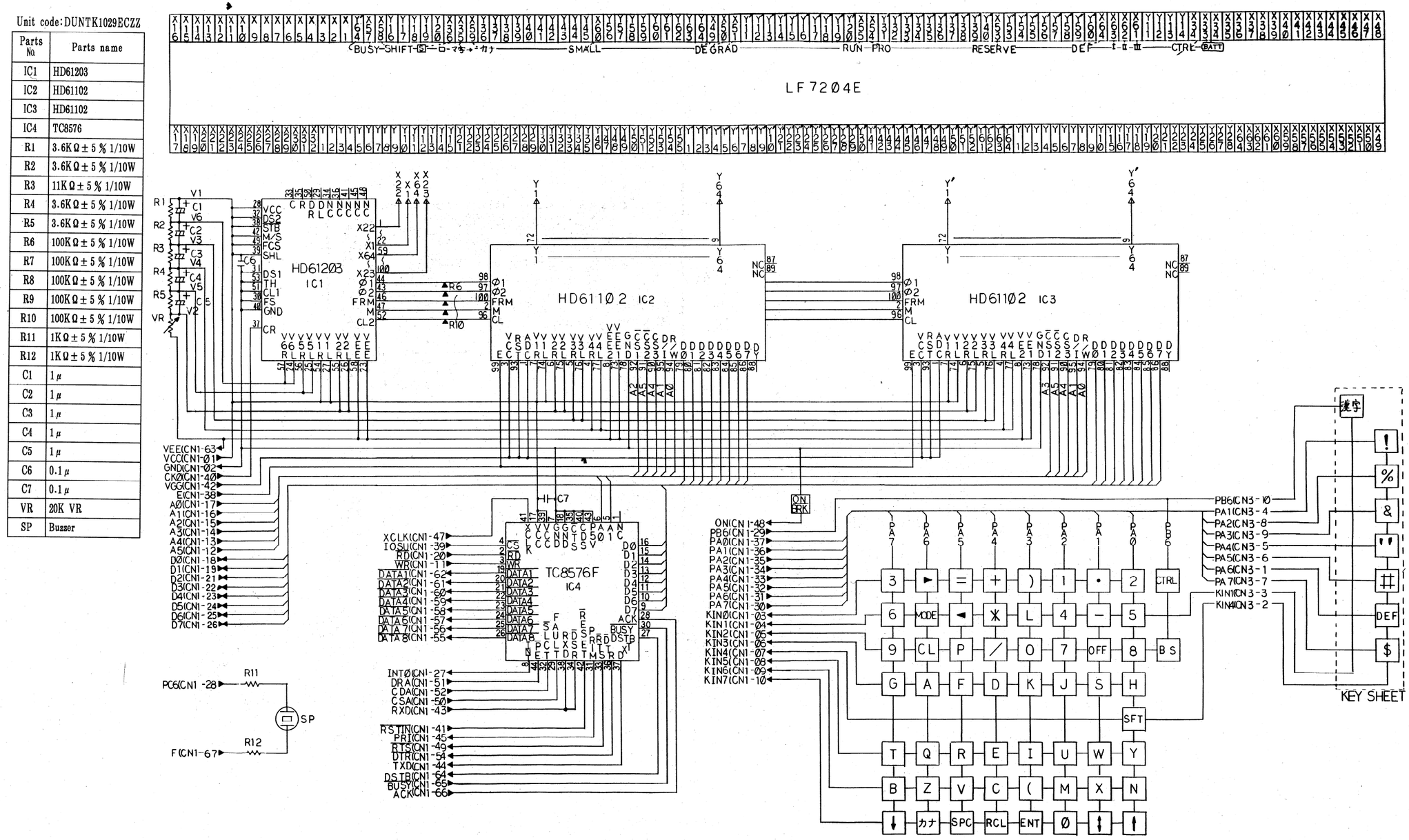
KEY P.W.B. (LSI SIDE)



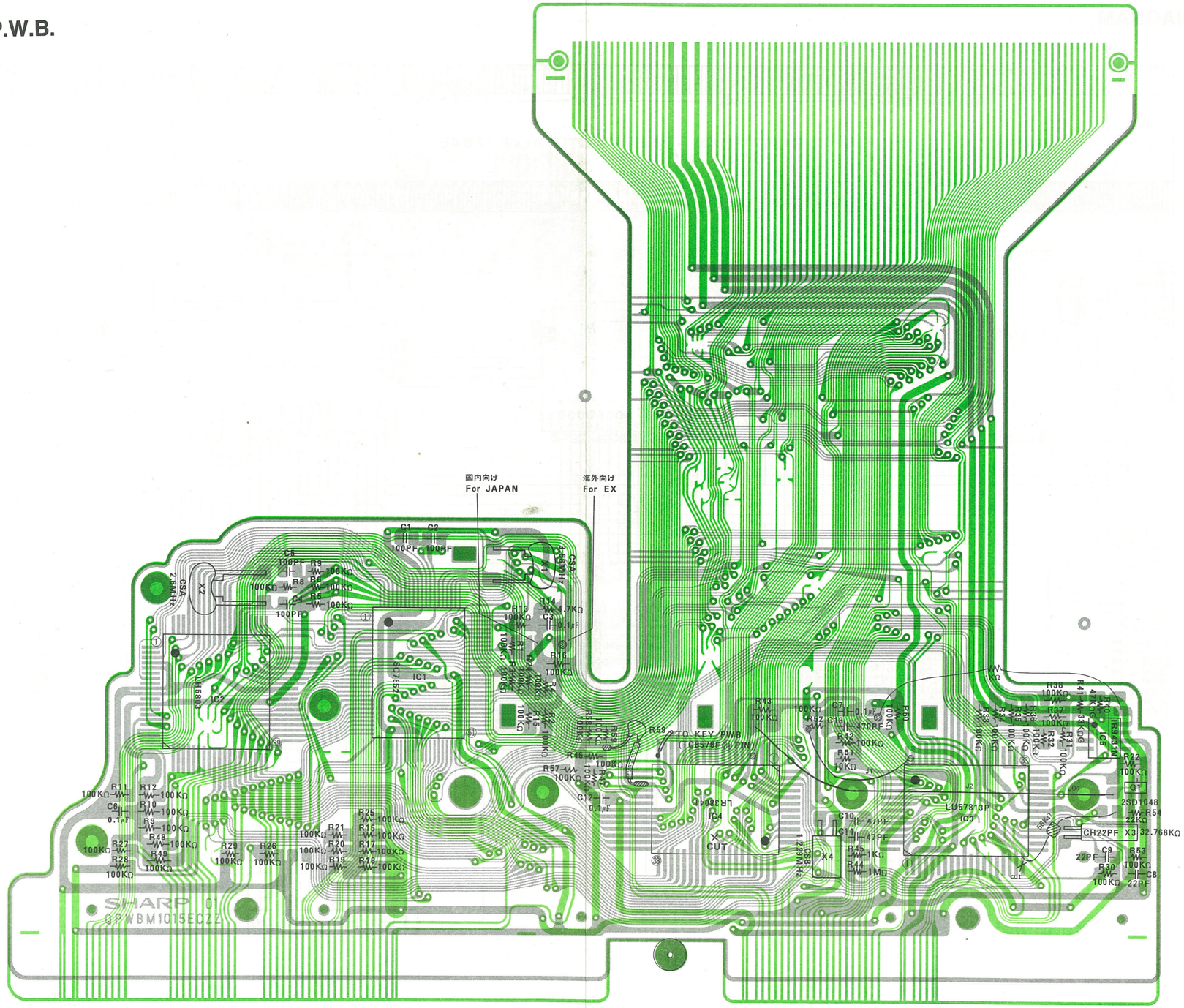
KEY CIRCUIT DIAGRAM

Unit code: DUNTK1029ECZZ

Parts No.	Parts name
IC1	HD61203
IC2	HD61102
IC3	HD61102
IC4	TC8576
R1	3.6KΩ ± 5 % 1/10W
R2	3.6KΩ ± 5 % 1/10W
R3	11KΩ ± 5 % 1/10W
R4	3.6KΩ ± 5 % 1/10W
R5	3.6KΩ ± 5 % 1/10W
R6	100KΩ ± 5 % 1/10W
R7	100KΩ ± 5 % 1/10W
R8	100KΩ ± 5 % 1/10W
R9	100KΩ ± 5 % 1/10W
R10	100KΩ ± 5 % 1/10W
R11	1KΩ ± 5 % 1/10W
R12	1KΩ ± 5 % 1/10W
C1	1 μ
C2	1 μ
C3	1 μ
C4	1 μ
C5	1 μ
C6	0.1 μ
C7	0.1 μ
VR	20K VR
SP	Buzzer



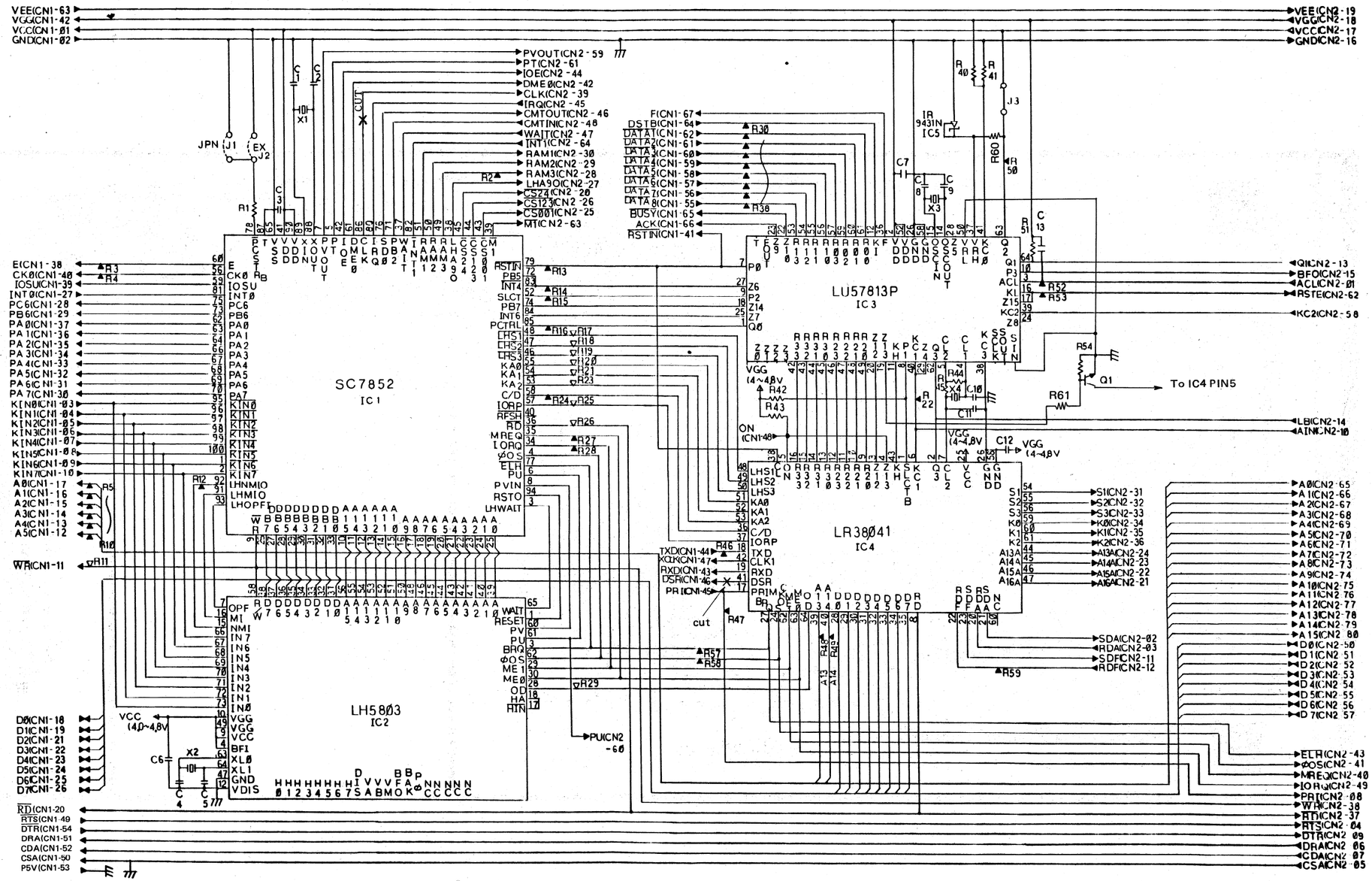
F.P.C. P.W.B.


国内向け
For JAPAN
海外向け
For EX
C1
C2
100PF
100PF
C5
100PF
R3
100KΩ
R4
100KΩ
R5
100KΩ
R6
100KΩ
C1
100PF
X2
C3A
R13
100KΩ
R14
4.7KΩ
C3
R16
100KΩ
IC1
IC2
R59
2 TO KEY P.W.B
(TC8578F)
R46
100KΩ
R57
100KΩ
C12
0.1μF
R43
100KΩ
R7
100KΩ
C7
0.1μF
C10
47PF
C11
47PF
IC3
R45
1KΩ
R44
1MΩ
X4
CUT
R38
100KΩ
R37
100KΩ
R36
100KΩ
R35
100KΩ
R34
100KΩ
R33
100KΩ
R32
100KΩ
R31
100KΩ
R42
100KΩ
R51
10KΩ
R52
100KΩ
2SD1048
R54
2KΩ
CH22PF
X3
32.768KΩ
C9
22PF
R53
100KΩ
R30
100KΩ
C8
22PF
R11
100KΩ
R12
100KΩ
R10
100KΩ
R3
100KΩ
R48
100KΩ
R49
100KΩ
C6
0.1μF
R27
100KΩ
R28
100KΩ
R29
100KΩ
R26
100KΩ
R21
100KΩ
R20
100KΩ
R19
100KΩ
R25
100KΩ
R15
100KΩ
R17
100KΩ
R16
100KΩ
SHARP 01
PWBM1015ECZZ

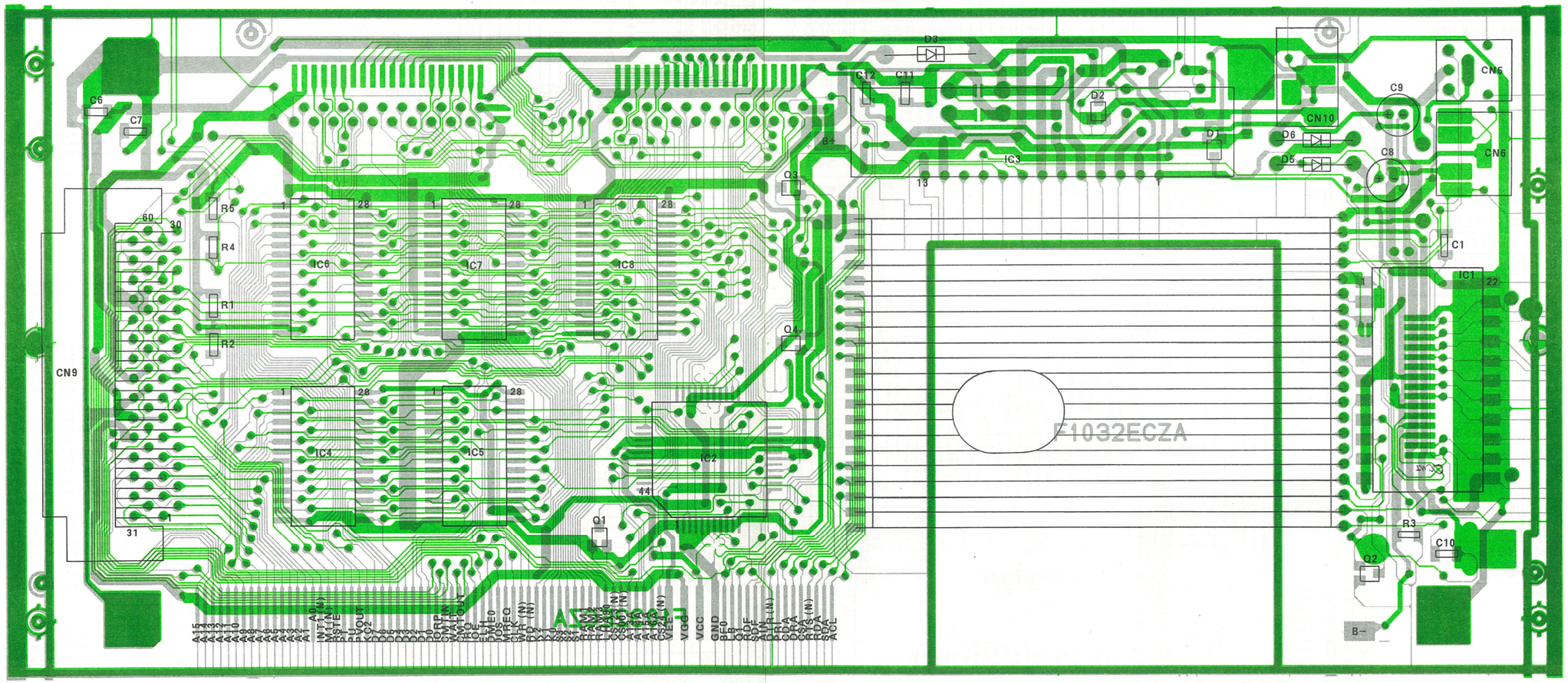
F.P.C. CIRCUIT DIAGRAM

Unit code: DUNTK1035ECZZ

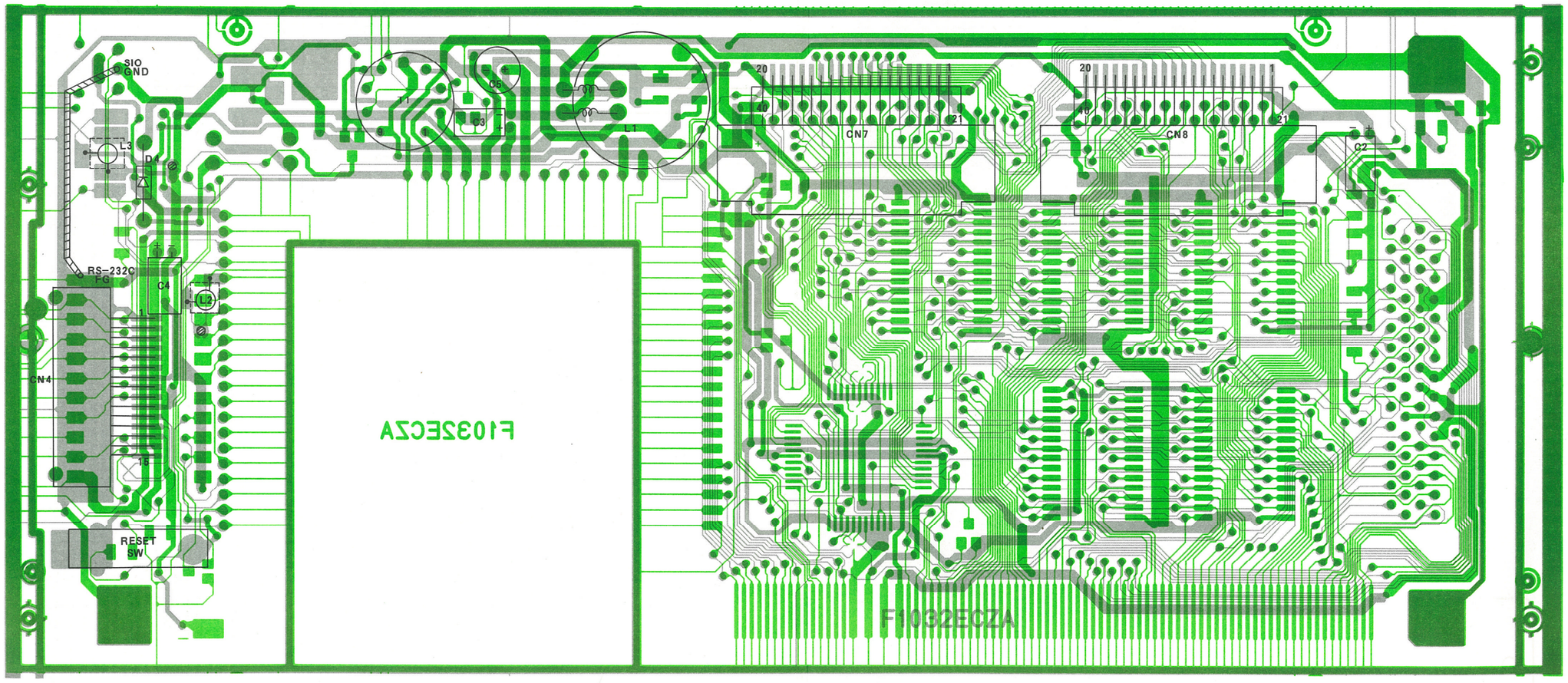
Parts No.	Parts name
IC1	SC7852
IC2	LH5803
IC3	LU57813P
IC4	LR38041
IC5	IR9431N
R1~13	100KΩ ± 5 % 1/10W
R14	4.7KΩ ± 5 % 1/10W
R15~38	100KΩ ± 5 % 1/10W
R40	47KΩ ± 2 % 1/10W
R41	33KΩ ± 2 % 1/10W
R42,43	100KΩ ± 5 % 1/10W
R44	1MΩ ± 5 % 1/10W
R45	1KΩ ± 5 % 1/10W
R46~50	100KΩ ± 5 % 1/10W
R51	10KΩ ± 5 % 1/10W
R52,53	100KΩ ± 5 % 1/10W
R54	22KΩ ± 5 % 1/10W
R57~59	100KΩ ± 5 % 1/10W
C1,2	100P ± 5 % CH50V
C3	0.1μ %
C4,5	100P ± 5 % CH50V
C6,7	0.1μ %
C8,9	22P ± 5 % CH50V
C10,11	47P ± 5 % CH50V
C12	0.1μ %
C13	470F
X1	CSA series 3.58M
X2	CSA series 2.6M
X3	Covered by shrinking tube 3×8 type 32.768K
X4	CSB series 1.229M
Q1	2SD1048
R60	1KΩ ± 5 %¼W
R61	56KΩ ± 5 %¼W



CONNECTOR P.W.B.



CONNECTOR P.W.B.



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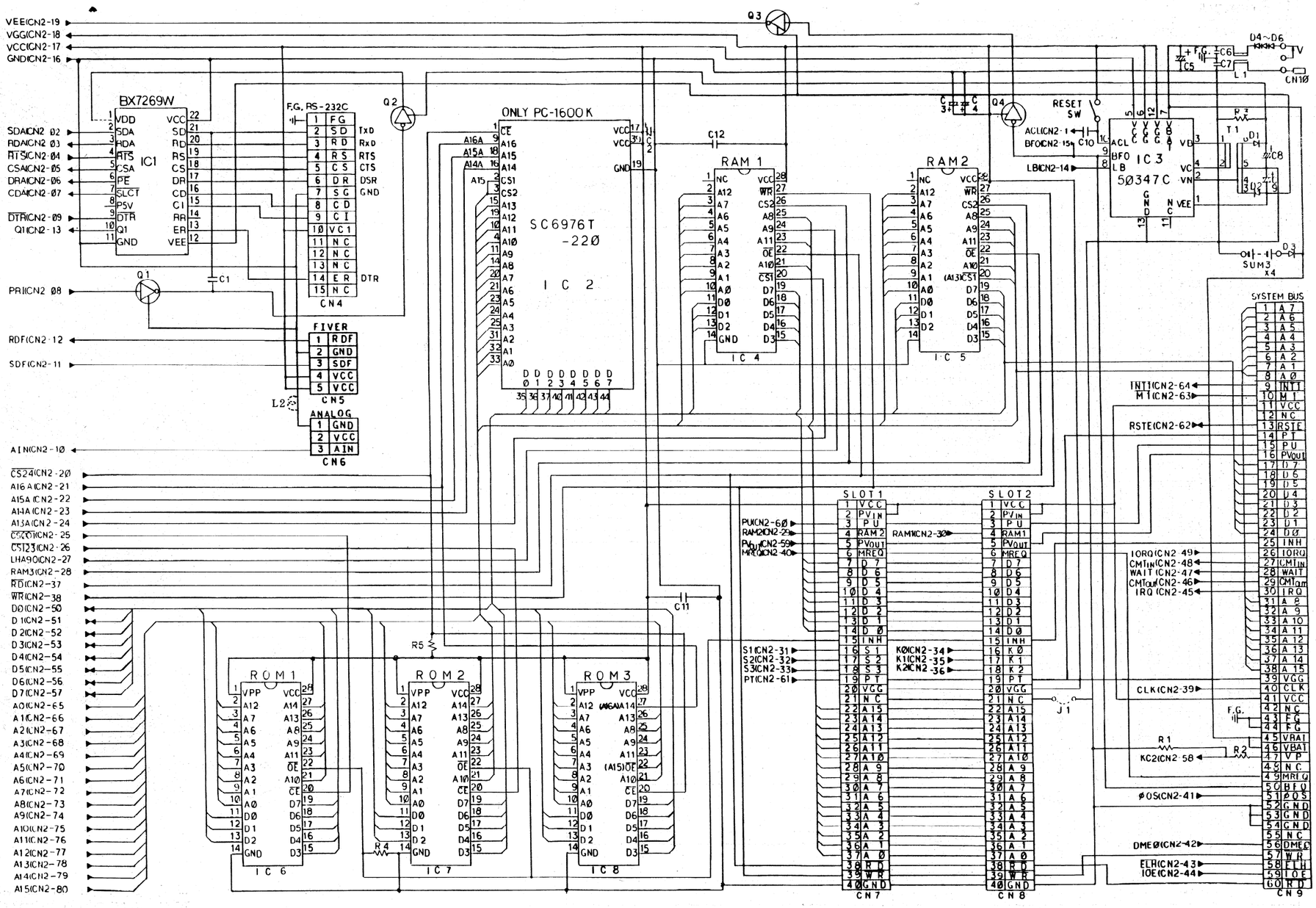
CONNECTOR CIRCUIT DIAGRAM

Unit code : DUNTK1071ECZA

Parts No.	Parts name
IC1	Hybrid IC2
IC2	Not used
IC3	Hybrid IC1
IC4	64K S-RAM
IC5	64K R-RAM
IC6	IC ROM1
IC7	IC ROM2
IC8	IC ROM3
Q1	Digitral transistor(144M)
Q2	Digitral transistor(114YM)
Q3	Digitral transistor(144M)
Q4	Digitral transistor(114YM)
R1	15KΩ(chip)
R2	33KΩ(chip)
R3	22KΩ(chip)
R4	100KΩ(chip)
R5	10KΩ(chip)
C1	470P(chip)
C2	6.3V 47μ
C3	6.3V 22μ
C4	6.3V 22μ
C5	10V 47μ
C6	0.1μ(chip)
C7	0.1μ(chip)
C8	10V 22μ
C9	10V 22μ
C10	0.01μ(chip)
C11	0.1μ(chip)
C12	0.1μ(chip)
T1	Converter transformer
L1	Noise filter
D1	DAN202
D2	DAP202
D3	11DQ03
D4	10E1N
D5	10E1N
D6	10E1N
SW	Reset SW
CN4	RS-232C
CN5	FIVER
CN6	ANALOG
CN7	SLOT1
CN8	SLOT2
CN9	SYSTEM BUS
CN10	Adaptor
L2	Filter coil
L3	Filter coil



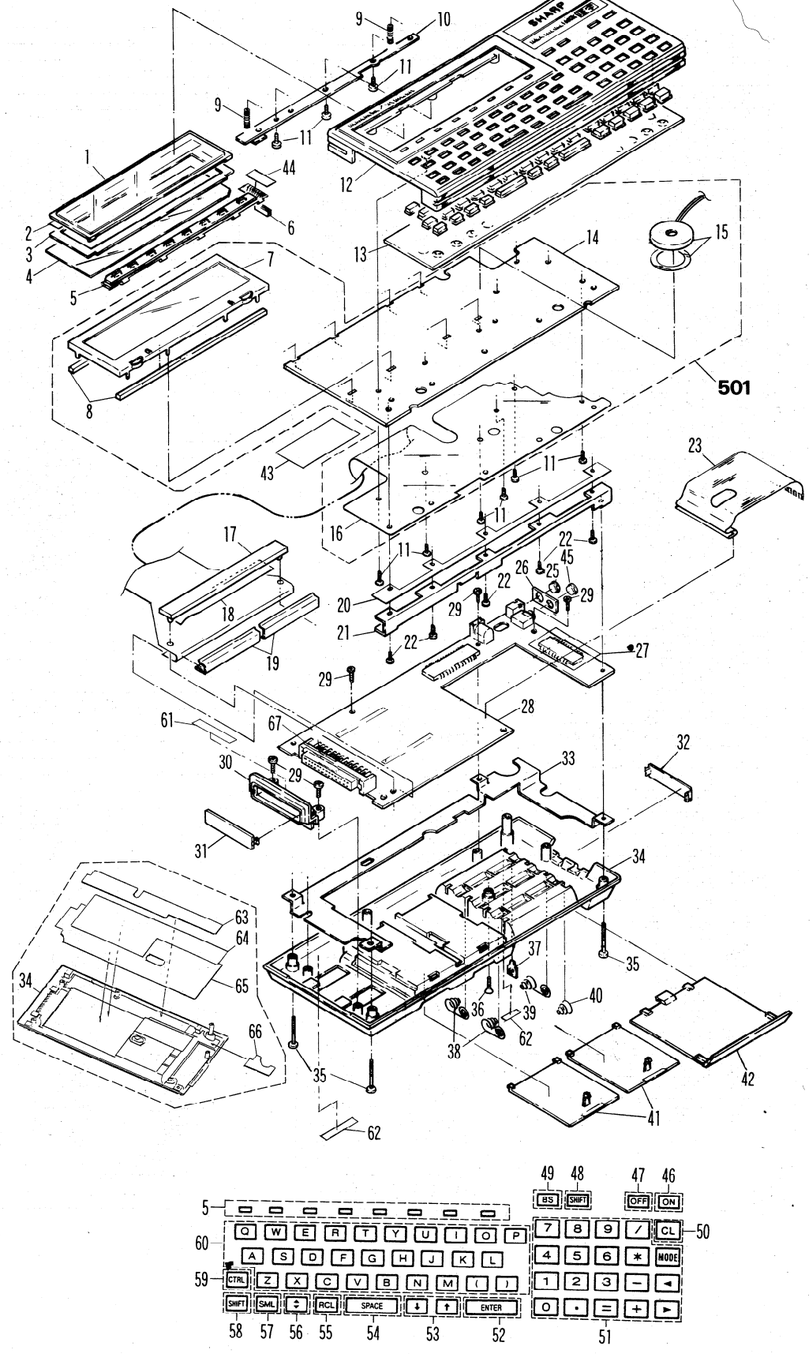
12. PARTS LIST & GUIDE

1 Exteriors

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	PFiLW1004ECZZ	AC	N	C	Acryl filter
2	PTPEH1014CCZZ	AA		C	FPC fixing tape
3	PSLDP1003ECZZ	AC	N	C	Display mask
4	PFiLV1005ECZZ	AE	N	C	Polarized filter
5	DUNT−1031ECZZ	AR	N	E	Soft key unit
6	PGUMS1004ECZZ	AA	N	B	Rubber connector
7	DUNT−1063ECZZ	AY	N	E	LCD unit
8	PGUMS1550CCZZ	AC		C	PWB−LCD connector
9	MSPRC1003ECZZ	AC	N	C	Static spring A
10	LANGT1001ECZZ	AD	N	C	Angle A
11	LX−BZ1147CCZZ	AA		C	Screw
12	DUNTG1037ECZZ	AS	N	D	Top cabinet unit (This includes No.44)
13	PGUMM1003ECZZ	AK	N	B	Spring rubber
14	DUNTK1029ECZZ	BY	N	E	Key PWB unit (This includes No.7,8,15)
15	RALMB1001ECZZ	AF	N	B	Buzzer
16	DUNTK1035ECZZ	BL	N	E	FPC PWB unit
17	LFiX−1001ECZZ	AB	N	C	FPC fixing plate
18	PSHEP1005ECZZ	AA	N	C	Protect sheet
19	LANGK1221CCZZ	AD		C	LCD fixing angle
20	PZETL1004ECZZ	AB	N	C	Insulator sheet
21	LANGT1002ECZZ	AD	N	C	Angle B
22	LX−BZ1184CCZZ	AA		C	Screw
23	QCNW−1001ECZZ	AD		C	Jumper wire
25	PCAPH1001ECZZ	AB	N	C	Protect cap
26	GCABC1008ECZZ	AB	N	D	Connector cabinet
27	PZETL1015ECZZ	AB	N	C	Insulator sheet A
28	DUNTK1071ECZA	CB	N	E	Connector PWB unit (USA, Germany)
	DUNTK1071ECZZ	CB	N	E	Connector PWB unit (Other countries)
29	XUBSD20P05000	AA		C	Screw (2×5)
30	GWAKP1041CCZZ	AF		C	Connector frame
31	GFTAA1267CCZZ	AC		D	Connector cover
32	GFTAA1287CC04	AB		D	Connector cover
33	PSLDC1004ECZZ	AH	N	C	Shield plate
34	GCABA1001ECZA	AE	N	D	Bottom cabinet
35	LX−BZ1006ECZZ	AA	N	C	Screw
36	XBSSD20P08000	AA		C	Screw
37	QTANZ1186CCZZ	AA		B	Battery terminal (⊕)
38	QTANZ1362CCZZ	AA		B	Battery terminal (⊕,⊖)
39	QTANZ1363CCZZ	AA		B	Battery terminal (⊕,⊖)
40	QTANZ1055CCZZ	AA		B	Battery terminal (⊖)
41	GFTAU1268CCSA	AB	N	D	Module cover
42	GFTAB1004ECZZ	AC	N	D	Battery cover
43	PZETL1016ECZZ	AA	N	C	Insulator sheet B
44	PTPEH1013ECZZ	AA	N	C	Tape
45	PCAPH1003ECZZ	AB	N	C	ANALOG in cap
46	JKNBZ1493CCZA	AE	N	C	Key top (ON key) (30PCS/1set)
47	JKNBZ1493CCZB	AE	N	C	Key top (OFF key) (30PCS/1set)
48	JKNBZ1493CCSA	AE	N	C	Key top (SHIFT key) (30PCS/1set)
49	JKNBZ1493CCSB	AE	N	C	Key top (BS key) (30PCS/1set)
50	JKNBZ1603CCSA	AE	N	C	Key top (CL key) (20PCS/1set)
51	JKNBZ1603CCSB	AE	N	C	Key top (Numeric and Arithmetic operation)
52	JKNBZ1732CCZA	AE	N	C	Key top (ENTER key) (10PCS/1set)
53	JKNBZ1492CCZE	AE	N	C	Key top (↑ ↓ key) (20PCS/1set)
54	JKNBZ1732CCSA	AE	N	C	Key top (SPACE key) (10PCS/1set)
55	JKNBZ1492CCZA	AE	N	C	Key top (RCL key) (20PCS/1set)
56	JKNBZ1492CCZD	AE	N	C	Key top (◆key) (20PCS/1set)
57	JKNBZ1492CCZB	AE	N	C	Key top (SML key) (20PCS/1set)
58	JKNBZ1492CCSB	AE	N	C	Key top (SHIFT key) (20PCS/1set)
59	JKNBZ1492CCSA	AE	N	C	Key top (CTRL key) (20PCS/1set)
60	JKNBZ1731CCSA	AF	N	C	Key top (Alphabetic keys)
61	PZETL1296CCZZ	AA		C	Sheet B
62	PSHEZ1015ECZZ	AA	N	C	Sheet
63	PSLDC1013ECZZ	AB	N	C	Shield plate B
64	PZETL1018ECZZ	AB	N	C	Insulator sheet
65	PSLDC1012ECZZ	AD	N	C	Shield plate A
66	PZETL1019ECZZ	AA	N	C	Insulator sheet
67	PCUSG1002ECZZ	AA	N	C	Cushion rabber
501	DUNT−1086ECZZ	CC	N	E	Key PWB+FPC PWB unit

2 Key PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	DUNT−1063ECZZ	AY	N	E	LCD unit
2	PGUMS1550CCZZ	AC		C	PWB−LCD connector
3	PSHEG1035CCZZ	AA		C	Sheet



2 Key PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
4	RALMB1001ECZZ	AF	N	B	Buzzer
5	RC-CZ1021CCZZ	AB		C	Capacitor (0.1μF)
6	RC-SZ1007CCZZ	AF		C	Capacitor (1μF)
7	RVR-Z2400QCN1	AF		B	Variable resistor (20KΩ)
8	VHiHD61102/-1	AX	N	B	IC (HD61102)
9	VHiHD61203/-1	AX	N	B	IC (HD61203)
10	VHiTC8576F/-1	AY	N	B	IC (TC8576F)
11	VRS-TP2BD102J	AA		C	Resistor (1/8W 1KΩ ±5%)
12	VRS-TP2BD104J	AA		C	Resistor (1/8W 100KΩ ±5%)
13	VRS-TP2BD113J	AA		C	Resistor (1/8W 11KΩ ±5%)
14	VRS-TP2BD362J	AA	N	C	Resistor (1/8W 3.6KΩ ±5%)
	(Unit)				
901	DUNTK1029ECZZ	BY	N	E	Key PWB unit

3 FPC PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
1	VHiSC7852//-1	BG	N	B	IC (SC7852)	[IC1]
2	VHiLH5803//-1	AY	N	B	IC (LH5803)	[IC2]
3	VHiLU57813P-1	AY	N	B	IC (LU57813P)	[IC3]
4	VHiLR38041/-1	AR	N	B	IC (LR38041)	[IC4]
5	VHiiR9431N/-1	AG	N	B	IC (IR9431N)	[IC5]
6	VRS-TV2AD104J	AA	N	C	Resistor (1/10W 100KΩ ±5%)	[R1~13,15~38,42,43]
	VRS-TV2AD104J	AA	N	C	Resistor (1/10W 100KΩ ±5%)	[R46~50,52,53,57~59]
7	VRS-TV2AD472J	AA	N	C	Resistor (1/10W 4.7KΩ ±5%)	[R14]
8	VRS-TV2AD473G	AA	N	C	Resistor (1/10W 47KΩ ±2%)	[R40]
9	VRS-TV2AD333G	AA	N	C	Resistor (1/10W 33KΩ ±2%)	[R41]
10	VRS-TV2AD105J	AA	N	C	Resistor (1/10W 1.0MΩ ±5%)	[R44]
11	VRS-TV2AD102J	AA	N	C	Resistor (1/10W 1.0KΩ ±5%)	[R45]
12	VRS-TV2AD103J	AA	N	C	Resistor (1/10W 10KΩ ±5%)	[R51]
13	VRS-TV2AD223J	AA	N	C	Resistor (1/10W 22KΩ ±5%)	[R54]
14	VRD-HT2EY102J	AA	N	C	Resistor (1/4W 1KΩ ±5%)	[R60]
15	VRD-HT2EY563J	AA	N	C	Resistor (1/4W 56KΩ ±5%)	[R61]
16	VCCCTV1H3101J	AA	N	C	Capacitor (50WV 100PF)	[C1,2,4,5]
17	RC-KZ2243YAZZ	AB	N	C	Capacitor (0.1μF)	[C3,6,7,12]
18	VCCCTV1H3220J	AA	N	C	Capacitor (50WV 22PF)	[[C8,9]
19	VCCCTV1H3470J	AA	N	C	Capacitor (50WV 47PF)	[C10,11]
20	VCCCTV1H3471J	AA	N	C	Capacitor (50WV 470PF)	[C13]
21	RCRSZ1002ECZZ	AF	N	B	Crystal (3.58MHZ)	[X1]
22	RCRSZ1038CCZZ	AE		B	Crystal (2.6MHZ)	[X2]
23	RCRSP1036CCZZ	AH		B	Crystal (32.768KHz)	[X3]
24	RCRSZ1001ECZZ	AE	N	B	Crystal (1.229MZ)	[X4]
25	RH-TX1014CCN1	AC		C	Transistor (2SD1048)	[Q1]
	(Unit)					
901	DUNTK1035ECZZ	BL	N	E	FPC PWB unit	

4 Connector PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	MSPRC1277CCZZ	AA		C	Connector spring (for 15pin connector)
2	PSHEZ1144CCZZ	AA		C	Nut fixing sheet (USA, Germany)
3	PSPAP1207CCZZ	AA		C	Connector spacer
4	PZETL1012ECZZ	AA	N	C	Battery insulator sheet
5	QCNCW1002EC0E	AK		C	Connector (5pin)
6	QCNCW1293CCZZ	AY		C	Connector (60pin)
7	QCNCW1294CCZZ	AX		C	Connector (40pin)
8	QCNCW1368CC1E	AM		C	Connector (15pin)
9	QCNTM1051CCZZ	AB		C	Reset terminal
10	QCNW-1001ECZZ	AD		C	Jumper wire
11	QJAKG1001ECZZ	AD	N	C	Jack (HST0861-440)
12	QJAKC1003CCZZ	AD		B	Jack for AC adaptor
13	QTANZ1004ECZZ	AA	N	C	Terminal
14	RC-CZ1021CCN1	AB		C	Capacitor (0.1μF)
15	RC-CZ1037CCN1	AB		C	Capacitor (0.01μF)
16	RC-CZ1038CCN1	AB		C	Capacitor (470pF)
17	RC-EZ226ACC0J	AB		C	Capacitor (6.3WV 22μF)
18	RC-EZ226ACC1A	AC		C	Capacitor (10WV 22μF)
19	RC-EZ476BCC0J	AB		C	Capacitor (6.3WV 47μF)
20	RC-EZ476BCC1A	AB		C	Capacitor (10WV 47μF)
21	RCiLZ1032CCZZ	AD		C	Coil (USA, Germany)
22	RH-DZ1005CCN1	AC		B	Diode (DAP202)
23	RH-DZ1008CCN1	AC		B	Diode (DAN202)

4 Connector PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
24	RFiLN1008CCZZ	AH		C	Filter (ESD−H−14B)
25	RTRNZ1001ECZZ	AE		B	Transformer
26	VHD10E1N///−1	AB		B	Diode (10E1N)
27	VHD11DQ03//−1	AE		B	Diode (11DQ03)
28	VHiBX7269W/−1	AV		B	IC (BX7269W)
29	VHiTC5565F15L	AW		B	IC (TC5565F15L)
30	VHi50347C//−1	AW		B	IC (50347C)
31	VHi53257F5212	AW	N	B	IC (53257F5212)
33	VHi53257F5213	AW	N	B	IC (53257F5213)
34	VHi53257F5214	AW	N	B	IC (53257F5214)
35	VRS−TP2BD103J	AA		C	Resistor (1/8W 10KΩ ±5%)
36	VRS−TP2BD104J	AA		C	Resistor (1/8W 100KΩ ±5%)
37	VRS−TP2BD153G	AA		C	Resistor (1/8W 15KΩ ±2%)
38	VRS−TP2BD223J	AA		C	Resistor (1/8W 22KΩ ±5%)
39	VRS−TP2BD333G	AA	N	C	Resistor (1/8W 33KΩ ±2%)
40	VSDTA114YM/−1	AC	N	B	Transistor (DTA114YM)
41	VSDTC144M//−1	AB	N	B	Transistor (DTC144M)
	(Unit)				
901	DUNTK1071ECZA	CB	N	E	Connector PWB unit (USA, Germany)
	DUNTK1071ECZZ	CB	N	E	Connector PWB unit (Other countries)

5 Packing material & Accessories

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	LPLTP1002ECZZ	AC	N	D	Top plate
2	LPLTP1003ECZZ	AC	N	D	Top plate 1
3	PSHEZ1014ECZZ	AE	N	C	Soft case sheet
	TiNSE1029ECZZ	AZ	N	D	Instruction book (USA)
4	TiNSG1031ECZZ	AZ	N	D	Instruction book (Germany)
	TiNSE1030ECZZ	AZ	N	D	Instruction book (English)
5	TCAUH1006ECZZ	AA	N	D	Caution card
6	UBAGC1290CCZZ	AR		D	Soft case
7	SPAKA0101ECZZ	AD	N	D	Packing cushion (Germany only)
8	SPAKA0045ECZZ	AK	N	D	Packing cushion
9	SPAKC0077ECZZ	AH	N	D	Packing case
10	PTPEZ1009ECZZ	AB	N	C	Double−side tape
11	TCAUH1001ECZZ	AB	N	C	Module caution card

■ Index

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
【D】					
DUNT-1031ECZZ	1- 5	AR	N	E	
DUNT-1063ECZZ	1- 7	AY	N	E	
//	2- 1	AY	N	E	
DUNT-1086ECZZ	1- 501	CC	N	E	
DUNTG1037ECZZ	1- 12	AS	N	D	
DUNTK1029ECZZ	1- 14	BY	N	E	
//	2- 901	BY	N	E	
DUNTK1035ECZZ	1- 16	BL	N	E	
//	3- 901	BL	N	E	
DUNTK1071ECZA	1- 28	CB	N	E	
//	4- 901	CB	N	E	
DUNTK1071ECZZ	1- 28	CB	N	E	
//	4- 901	CB	N	E	
【G】					
GCABA1001ECZA	1- 34	AE	N	D	
GCABC1008ECZZ	1- 26	AB	N	D	
GFTAA1267CCZZ	1- 31	AC		D	
GFTAA1287CC04	1- 32	AB		D	
GFTAB1004ECZZ	1- 42	AC	N	D	
GFTAU1268CCSA	1- 41	AB	N	D	
GWAKP1041CCZZ	1- 30	AF		C	
【J】					
JKNBZ1492CCSA	1- 59	AE	N	C	
JKNBZ1492CCSB	1- 58	AE	N	C	
JKNBZ1492CCZA	1- 55	AE	N	C	
JKNBZ1492CCZB	1- 57	AE	N	C	
JKNBZ1492CCZD	1- 56	AE	N	C	
JKNBZ1492CCZE	1- 53	AE	N	C	
JKNBZ1493CCSA	1- 48	AE	N	C	
JKNBZ1493CCSB	1- 49	AE	N	C	
JKNBZ1493CCZA	1- 46	AE	N	C	
JKNBZ1493CCZB	1- 47	AE	N	C	
JKNBZ1603CCSA	1- 50	AE	N	C	
JKNBZ1603CCSB	1- 51	AE	N	C	
JKNBZ1731CCSA	1- 60	AF	N	C	
JKNBZ1732CCSA	1- 54	AE	N	C	
JKNBZ1732CCZA	1- 52	AE	N	C	
【L】					
LANGK1221CCZZ	1- 19	AD		C	
LANGT1001ECZZ	1- 10	AD	N	C	
LANGT1002ECZZ	1- 21	AD	N	C	
LFiX-1001ECZZ	1- 17	AB	N	C	
LPLTP1002ECZZ	5- 1	AC	N	D	
LPLTP1003ECZZ	5- 2	AC	N	D	
LX-BZ1006ECZZ	1- 35	AA	N	C	
LX-BZ1147CCZZ	1- 11	AA		C	
LX-BZ1184CCZZ	1- 22	AA		C	
【M】					
MSPRC1003ECZZ	1- 9	AC	N	C	
MSPRC1277CCZZ	4- 1	AA		C	
【P】					
PCAPH1001ECZZ	1- 25	AB	N	C	
PCAPH1003ECZZ	1- 45	AB	N	C	
PCUSG1002ECZZ	1- 67	AA	N	C	
PFiLV1005ECZZ	1- 4	AE	N	C	
PFiLW1004ECZZ	1- 1	AC	N	C	
PGUMM1003ECZZ	1- 13	AK	N	B	
PGUMS1004ECZZ	1- 6	AA	N	B	
PGUMS1550CCZZ	1- 8	AC		C	
//	2- 2	AC		C	
PSHEG1035CCZZ	2- 3	AA		C	
PSHEP1005ECZZ	1- 18	AA	N	C	
PSHEZ1014ECZZ	5- 3	AE	N	C	
PSHEZ1015ECZZ	1- 62	AA	N	C	
PSHEZ1144CCZZ	4- 2	AA		C	
PSLDC1004ECZZ	1- 33	AH	N	C	
PSLDC1012ECZZ	1- 65	AD	N	C	
PSLDC1013ECZZ	1- 63	AB	N	C	
PSLDP1003ECZZ	1- 3	AC	N	C	
PSPAP1207CCZZ	4- 3	AA		C	
PTPEH1013ECZZ	1- 44	AA	N	C	
PTPEH1014CCZZ	1- 2	AA		C	
PTPEZ1009ECZZ	5- 10	AB	N	C	
PZETL1004ECZZ	1- 20	AB	N	C	
//	4- 4	AA	N	C	
PZETL1015ECZZ	1- 27	AB	N	C	
PZETL1016ECZZ	1- 43	AA	N	C	
PZETL1018ECZZ	1- 64	AB	N	C	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
PZETL1019ECZZ	1- 66	AA	N	C	
PZETL1296CCZZ	1- 61	AA		C	
【Q】					
QCNCW1002EC0E	4- 5	AK		C	
QCNCW1293CCZZ	4- 6	AY		C	
QCNCW1294CCZZ	4- 7	AX		C	
QCNCW1368CC1E	4- 8	AM		C	
QCNTM1051CCZZ	4- 9	AB		C	
QCNW-1001ECZZ	1- 23	AD		C	
//	4- 10	AD		C	
QJAKC1003CCZZ	4- 12	AD		B	
QJAKG1001ECZZ	4- 11	AD	N	C	
QTANZ1004ECZZ	4- 13	AA	N	C	
QTANZ1055CCZZ	1- 40	AA		B	
QTANZ1186CCZZ	1- 37	AA		B	
QTANZ1362CCZZ	1- 38	AA		B	
QTANZ1363CCZZ	1- 39	AA		B	
【R】					
RALMB1001ECZZ	1- 15	AF	N	B	
//	2- 4	AF	N	B	
RC-CZ1021CCN1	2- 5	AB		C	
//	4- 14	AB		C	
RC-CZ1037CCN1	4- 15	AB		C	
RC-CZ1038CCN1	4- 16	AB		C	
RC-EZ226ACC0J	4- 17	AB		C	
RC-EZ226ACC1A	4- 18	AC		C	
RC-EZ476BCC0J	4- 19	AB		C	
RC-EZ476BCC1A	4- 20	AB		C	
RC-KZ2243YAZZ	3- 17	AB	N	C	
RC-SZ1007CCZZ	2- 6	AF		C	
RCiLZ1032CCZZ	4- 21	AD		C	
RCRSP1036CCZZ	3- 23	AH		B	
RCRSZ1001ECZZ	3- 24	AE	N	B	
RCRSZ1002ECZZ	3- 21	AF	N	B	
RCRSZ1038CCZZ	3- 22	AE		B	
RFiLN1008CCZZ	4- 24	AH		C	
RH-DZ1005CCZZ	4- 22	AC		B	
RH-DZ1008CCZZ	4- 23	AC		B	
RH-TX1014CCN1	3- 25	AC		C	
RTRNZ1001ECZZ	4- 25	AE		B	
RVR-Z2400QCN1	2- 7	AF		B	
【S】					
SPAKA0045ECZZ	5- 8	AK	N	D	
SPAKA0101ECZZ	5- 7	AD	N	D	
SPAKC0077ECZZ	5- 9	AH	N	D	
【T】					
TCAUH1001ECZZ	5- 11	AB	N	C	
TCAUH1006ECZZ	5- 5	AA	N	D	
TiNSE1029ECZZ	5- 4	AZ	N	D	
TiNSE1030ECZZ	5- 4	AZ	N	D	
TiNSG1031ECZZ	5- 4	AZ	N	D	
【U】					
UBAGC1290CCZZ	5- 6	AR		D	
【V】					
VCCCTV1H3101J	3- 16	AA	N	C	
VCCCTV1H3220J	3- 18	AA	N	C	
VCCCTV1H3470J	3- 19	AA	N	C	
VCCCTV1H3471J	3- 20	AA	N	C	
VHD10E1N///-1	4- 26	AB		B	
VHD11DQ03//-1	4- 27	AE		B	
VHiBX7269W/-1	4- 28	AV		B	
VHiHD61102/-1	2- 8	AX	N	B	
VHiHD61203/-1	2- 9	AX	N	B	
VHiiR9431N/-1	3- 5	AG	N	B	
VHiLH5803//-1	3- 2	AY	N	B	
VHiLR38041/-1	3- 4	AR	N	B	
VHiLU57813P-1	3- 3	AY	N	B	
VHiSC7852//-1	3- 1	BG	N	B	
VHiTC5565F15L	4- 29	AW		B	
VHiTC8576F/-1	2- 10	AY	N	B	
VHi50347C//-1	4- 30	AW		B	
VHi53257F5212	4- 31	AW	N	B	
VHi53257F5213	4- 33	AW	N	B	
VHi53257F5214	4- 34	AW	N	B	
VRD-HT2EY102J	3- 14	AA	N	C	
VRD-HT2EY563J	3- 15	AA	N	C	
VRS-TP2BD102J	2- 11	AA		C	
VRS-TP2BD103J	4- 35	AA		C	
VRS-TP2BD104J	2- 12	AA		C	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
VRS－TP2BD104J	4- 36	AA		C	
VRS－TP2BD113J	2- 13	AA		C	
VRS－TP2BD153G	4- 37	AA		C	
VRS－TP2BD223J	4- 38	AA		C	
VRS－TP2BD333G	4- 39		N	C	
VRS－TP2BD362J	2- 14	AA	N	C	
VRS－TV2AD102J	3- 11	AA	N	C	
VRS－TV2AD103J	3- 12	AA	N	C	
VRS－TV2AD104J	3- 6	AA	N	C	
〃	3- 6	AA	N	C	
VRS－TV2AD105J	3- 10	AA	N	C	
VRS－TV2AD223J	3- 13	AA	N	C	
VRS－TV2AD333G	3- 9	AA	N	C	
VRS－TV2AD472J	3- 7	AA	N	C	
VRS－TV2AD473G	3- 8	AA	N	C	
VSDTA114YM／－1	4- 40	AC	N	B	
VSDTC144M／／－1	4- 41	AB	N	B	
【X】					
XBBSD20P08000	4- 42	AA		C	
XBSSD20P08000	1- 36	AA		C	
XNESD20－16000	4- 43	AA		C	
XUBSD20P05000	1- 29	AA		C	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	

MODEL CE-1600P

• 4-color plotting printer

Table of contents

1. Specifications

Model name:
CE-1600P
Type:
Printer/cassette interface
Print method:
X-Y plotting
Print capacity:
160 printing positions/line (with minimum size print characters)
Printing colors:
Four colors of black, blue, green, and red
Printing character size:
Nine sizes (0.8 mm x 1.2 mm ~ 7.2 mm x 10.8 mm).
Printing directions:
Four directions.
Minimum print pen moving distance:
0.2 mm
Printing speed:
5 characters/second, average (printing the size 2 characters in black with all kinds of ASCII characters (96)).
The printing speed is subject to variation depending on the print contents and program.
Print form:
210 mm wide roll paper whose roll size is up to 40 mm (EA-4AR1).
216 mm wide roll paper (EA-1LR1).
Cut sheet (A4 or letter size)
Power supply:
From the internal rechargeable batteries which can be recharged through the AC adaptor (EA-160).
Power consumption:
6VDC , 5.7W
Maximum printable lines per charge:
About 250 lines after 8 hours of recharge (continuous printing 40 digits of "5" of the print size 2 in black on a single line under the operating temperature of 20°C).
Operating temperature:
5°C ~ 40°C
Physical dimensions:
320 mm (W) x 221.5 mm (D) x 46 mm (H)
Weight:
About 1.6 kg including the pocket.
Accessories:
EA-160 AC adaptor, hard case, roll paper (1 pc), pen (2 pcs each of black, blue, green, and red), tape recorder interfacing cable (1 pc), paper holder (1 set), shaft (1 pc), instruction book

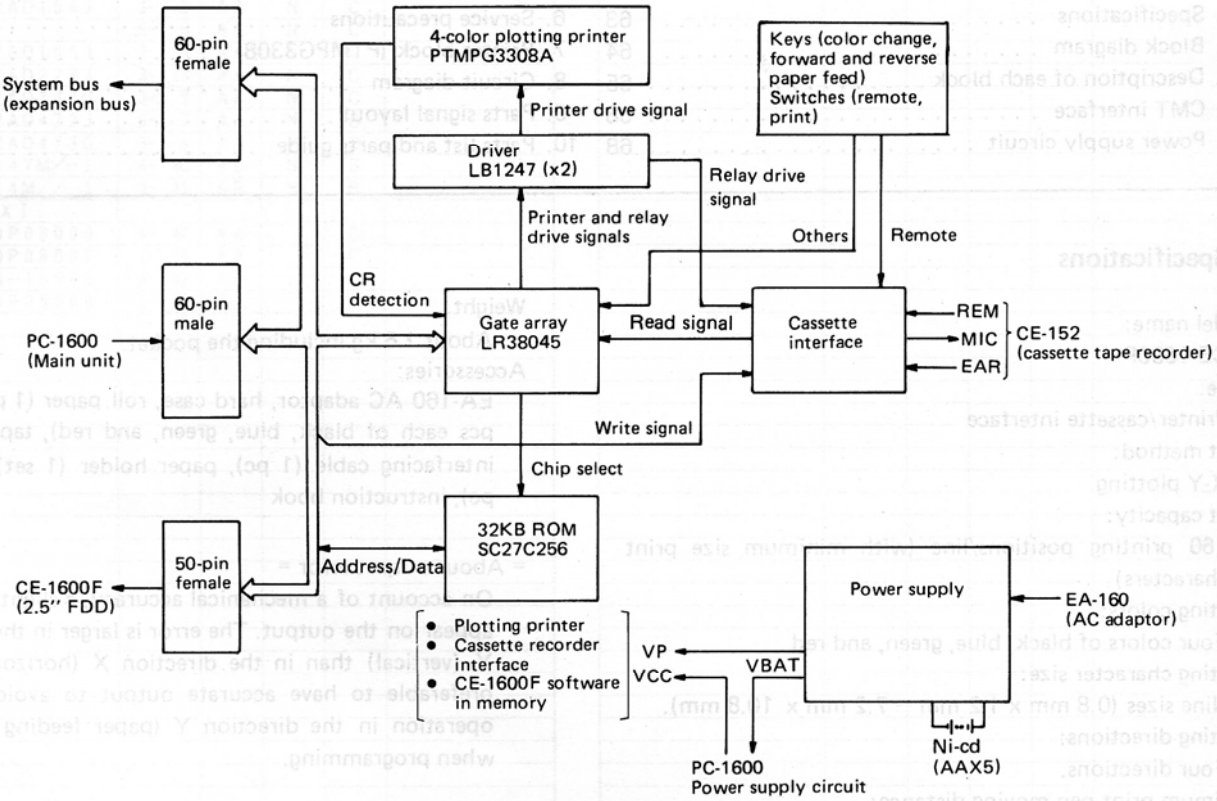
= About output error =
On account of a mechanical accuracy, a slight error may appear on the output. The error is larger in the direction Y (vertical) than in the direction X (horizontal). It is preferable to have accurate output to avoid repeated operation in the direction Y (paper feeding direction) when programming.

Options
The following options are available for the CE-1600P.

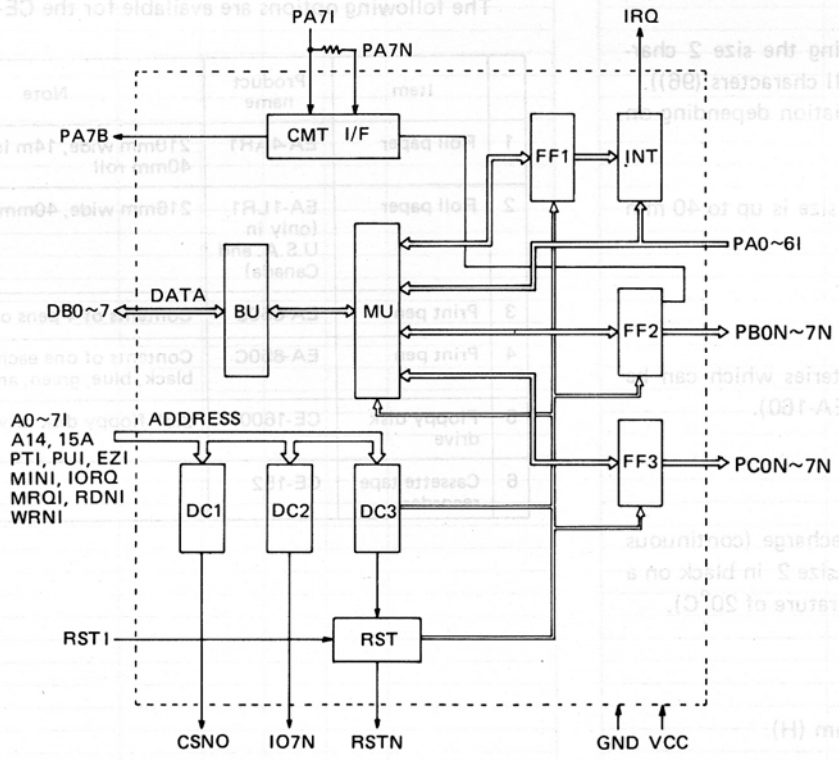
	Item	Product name	Note
1	Roll paper	EA-4AR1	210mm wide, 14m long, 40mm roll
2	Roll paper	EA-1LR1 (only in U.S.A. and Canada)	216mm wide, 40mm roll
3	Print pen	EA-850B	Contents of 4 pens of black.
4	Print pen	EA-850C	Contents of one each pen of black, blue, green, and red.
5	Floppy disk drive	CE-1600F	2.5" floppy disk drive unit
6	Cassette tape recorder	CE-152	

2. Block diagram

Since the printer, cassette, and floppy disk drive are all controlled by the PC-1600, the CE-1600P and PC-1600F can not operate by itself.
Battery, however, can be recharged without intervention of the PC-1600.
A 32KB ROM within the CE-1600P contains the program to operate the printer, cassette, and floppy disk drive.



(Fig.1) CE-1600P block diagram



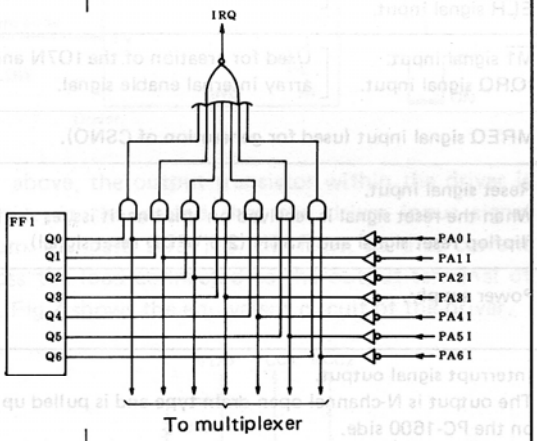
Bu:	8 bits I/O Buffer
Mu:	Multiplexer
FF1~3:	8 bits Latch
DC1~3:	Decorder
INT:	Interrupt circuit
RST:	Reset circuit
CMT I/F:	Serial input
PA0~7I:	8 bits input
PA0N~7N:	8 bits output port
PC0N~7N:	8 bits output port

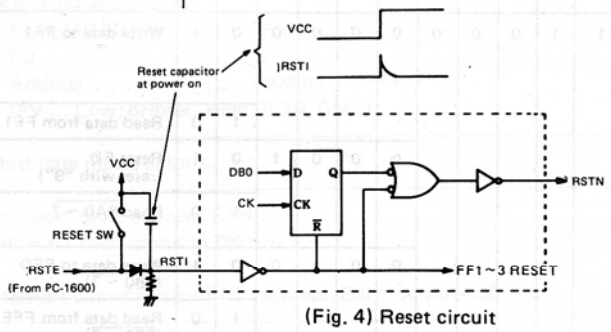
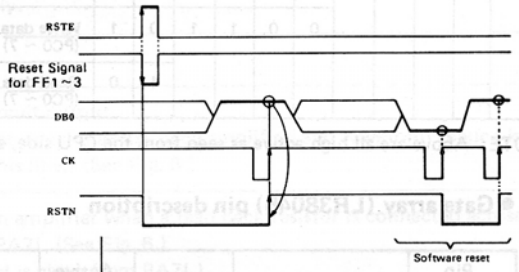
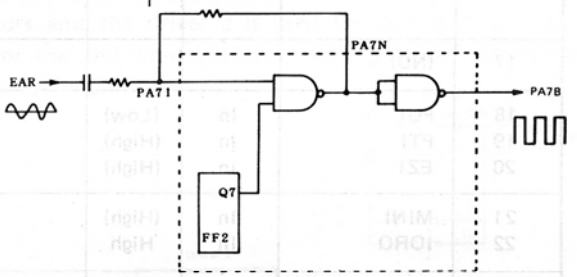
(Fig.1) LR38045 gate array block diagram

3. Description of each block

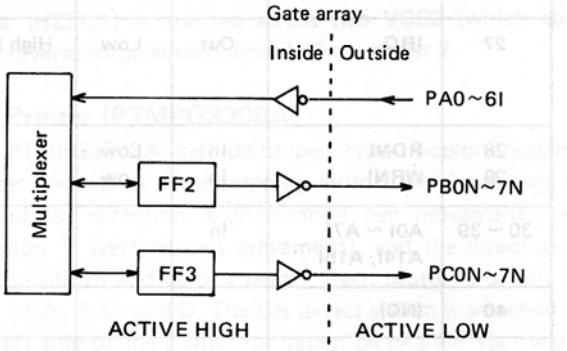
3-1. LR38045 gate array

Table below shows the functions and port address of the gate array block.

Block	Function
Bu (8-bit I/O buffer)	A bidirectional 8-bit input/output buffer.
Mu (multiplexer)	Used to select FF1, FF2, FF3, or PA port when data are read from the gate array.
FF1~FF3 (8-bit latch)	FF1: The interrupt circuit is controlled with an FF1 output. For instance, when a certain bit is set to "1", the input signal to the PA port (PA0~61) which corresponds to the bit is sent on the IRQ line as an interrupt signal. FF2: PB port (PB0~7N) latch FF3: PC port (PC0~7N) latch
DC1~3 (decoder)	DC1: For generation of 32KB ROM chip select signal. (CSNO) DC2: For generation of 2.5" FDD select signal. (IO7N) DC3: For selection of FF1~FF3 and FFD reset latch at the time of data write. Or selection of FF1~FF3 or PA port at the time of data read.
INT (interrupt circuit)	Inputs to the PA port (PA0~61) are ORed and sent on the IRQ line as an interrupt signal. As PA0~61 correspond to Q0~Q6 of FF1, the interrupt is enabled when FF1 is set with "1". (Fig. 3 shows the quivalent circuit of the interrupt circuit.)
	 (Fig. 3) Interrupt circuit
RST (reset circuit)	FF1~3 are reset by this circuit, when a reset signal is received on RSTI. At the same time, the 2/5" FDD reset signal (RSTN) is issued which will be kept active until cleared by software.

Block	Function
	It is possible without an input on RSTI to output RSTN by means of software. (Fig. 4 shows the equivalent circuit of the reset circuit and Fig. 5 shows its timings.)
	 (Fig. 4) Reset circuit  (Fig. 5) Reset circuit timings
CMT I/F (cassette interface circuit)	The cassette signal received from the EAR jack is amplified and waveform shaped, to be sent on PA7B. (See Fig.6 for its equivalent circuit.)
	 (Fig. 6) Cassette interface circuit equivalent circuit

NOTE: Ports, PA, PB, and PC, are all active high within the gate array, but they are converted to active low signals outside of the gate array.



For instance, if "1" is set to Q0 of FF2, the PB0N output becomes low.

TABLE-3

Port address

Table-1

IORQ	Address								WR	RD	Operation	Data							
M1	A7	A6	A5	A4	A3	A2	A1	A0				D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	0	0	0	0	0	0	1	Write data to FF1	0	*	Printer CR INT Enable	Printer SW INT Enable	FD INT Enable	Reverse PF key INT Enable	PF key INT Enable	CC key INT Enable
									1	0	Read data from FF1	↑	↑	↑	↑	↑	↑	↑	↑
					0	0	0	1	0	1	Reset FD (reset with "0")								FD Reset
									1	0	Read $\overline{PA0 \sim 7}$	CMT input	(0)	Printer CR	Print SW	FD INT	Reverse PF key	PC key	CC key
					0	0	1	0	0	1	Write data to FFD ($\overline{PB0 \sim 7}$)	CMT in Enable	*	RMT OFF	RMT ON	Motor ZD	Motor ZB	Motor ZC	Motor ZA
									1	0	Read data from FFE ($\overline{PB0 \sim 7}$)	↑	↑	↑	↑	↑	↑	↑	↑
					0	0	1	1	0	1	Write data to FFE ($\overline{PC0 \sim 7}$)	Motor YD	Motor YB	Motor YC	Motor YA	Motor XD	Motor XB	Motor XC	Motor XA
									1	0	Read data from FF3 ($\overline{PC0 \sim 7}$)	↑	↑	↑	↑	↑	↑	↑	↑

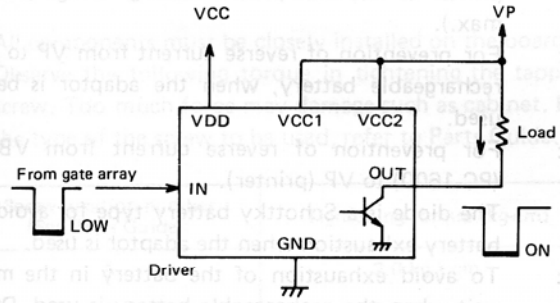
NOTE: Above are all high active as seen from the CPU side, except that FD reset is low active.

• Gate array (LR38045) pin description

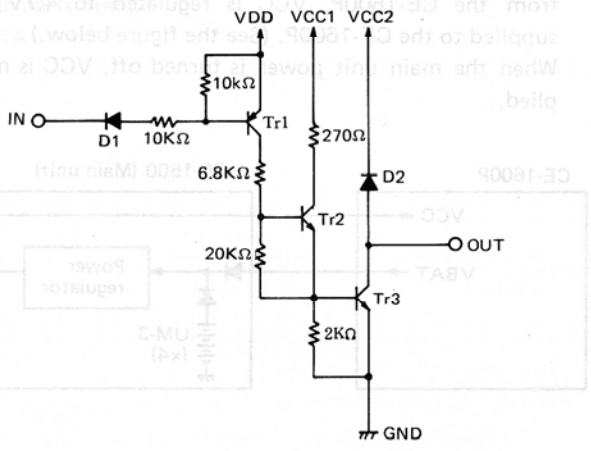
Pin No.	Symbol	I/O	Active level	Level at reset	Description
1 ~ 8	PC7N ~ PC0N	Out	Low	High	8-bit output port (port address: 83H). D0 ~ D7 correspond to PC0 ~ 7N via FF3'
9 ~ 16	PB7N ~ PB0N	Out	Low	High	8-bit output port (port address: 82H). D0 ~ D7 correspond to PB0 ~ 7N via FF2.
17	(NC)				
18 19 20	PUI PTI EZI	In In In	(Low) (High) (High)		PU signal input. PT signal input. $\overline{ELH}$ signal input. [Used for creation of a 32KB ROM signal (CSNO).]
21 22	MINI IORQ	In In	(High) High		$\overline{M1}$ signal input. IORQ signal input. [Used for creation of the IO7N and gate array internal enable signal.]
23	MRQI	In	High		MREQ signal input (used for generation of CSNO).
24	RSTI	In	High		Reset signal input. When the reset signal is received on this line, it issues the internal flipflop reset signal and RSTN (2.5" FDD reset signal).
25 26	VCC GND				Power supply.
27	IRQ	Out	Low	High impedance	Interrupt signal output. The output is N-channel open drain type and is pulled up to VCC on the PC-1600 side.
28 29	RDNI WRNI	In In	Low Low		$\overline{RD}$ signal input. $\overline{WR}$ signal input.
30 ~ 39	A0I ~ A7I A14I, A15I	In			Address input.
40	(NC)				
41	RSTN	Out	Low	Low	2.5" FDD reset signal output. The active state of the signal is unconditionally issued with a reset signal and it must be cleared by means of software. It is also possible to create the signal by software. (Address: 81H, D0, $\overline{WR}$)

Pin No.	Symbol	I/O	Active level	Level at reset	Description
42	IO7N	Out	Low	(High)	2.5" FDD select signal. (Out through the address 70H — 7FH)
43	CSNO	Out	Low	(High)	32KB ROM select signal. [$\overline{ELH}$, MREQ, PT . . . . . High PU . . . . . Low Address . . . . . 4000H ~ 7FFFH (PV ... Low; printer, High; FDD, CMT)]
44 ~ 51	DB0 ~ DB7	In/Out			(8-bit) data input/output.
52 ~ 57 60	PA01 ~ PA5I PA6I	In	Low		Input port (port address: 81H). (PA0 ~ 61 correspond to D0 ~ 6. (Interrupt controlled by FF1 (address: 80H) outputs Q0 ~ 6.)
58	GND				Power supply.
59	(NC)				
61	PA7B	Out	(High)	High	CMT I/F circuit output. (The cassette signal that has been amplified and waveform shaped is sent from this line.) (See Fig. 6.)
62 64	PA6N PA7I	(Out) In	(Low)	High	Comprise an amplifier when a feed back resistor is connected across PA7N and PA7I. (See Fig. 6.) (Input signal is given from PA7I.)
63	(NC)				

3-2. Printer drive IC (LB-1247)

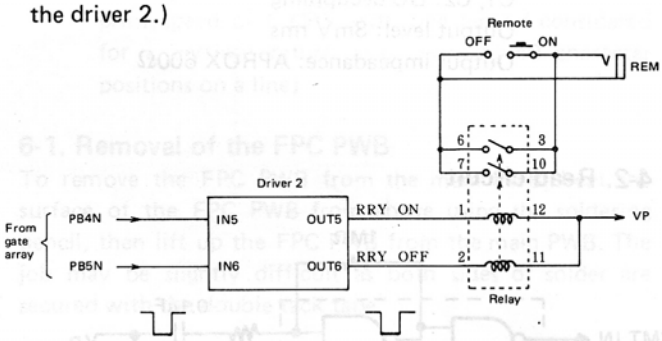


As shown above, the output transistor within the driver is turned active in the period that the driver input signal (signal from the gate array) is low level, so that current flows across the load connected to the output terminal of the driver. Fig.7 shows the equivalent circuit of the driver.



(Fig.7) Driver (LB1247) equivalent circuit

Eight circuits shown in Fig.7 are contained in a single driver circuit. The driver 1 is sued for driving of printer X and Z motors and the driver 2 is used for driving of printer Y motor and and remote relay. (Two circuits are not used for the driver 2.)



(Fig.8) Remote circuit

To increase the torque of the printer Y motor, a 5V zener diode (HZ5C1) is inserted across two VCC2 (which contains reverse surge absorb diode) of the driver 2.

3-3. Printer (PTMPG3308A)

The PTMPG3308A ball point pen type, 4-color, plotting printer consists of three stepping motors which are used to control the direction X (horizontal pen movement), the direction Y (vertical pen movement), and the direction Z (pen up/down and color change). Each motor is driven by coils of A, B, C, and D. The CR detect switch is attached to the left side of the printer for detection of a CR via the pin PA5I of the gate array. The X and y motors are 1-2 phase excited and the Z motor 2-2 phase excited.

See Section 7, Printer, for detail of PTMPG3308A printer specifications, characteristics, drive method, etc.

4. CMT interface

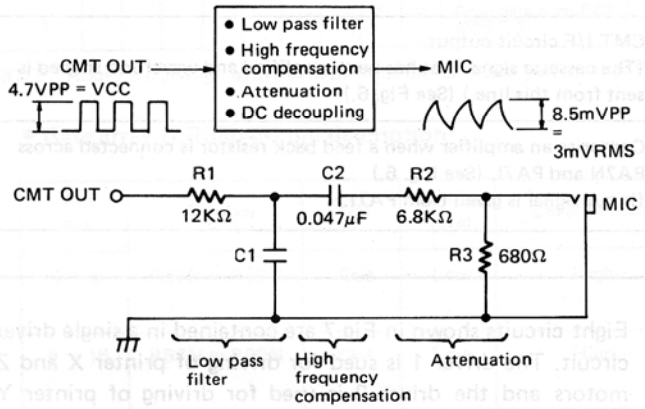
The CMT interface consists of the following circuits:

- Write circuit
- Read circuit
- Remote circuit

4-1. Write circuit

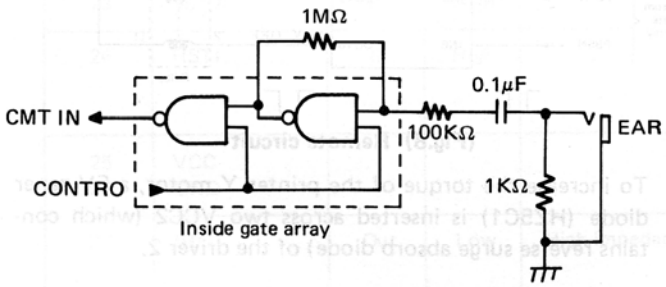
As shown below, the logic level signals are converted into signals of micro level.

- High frequency component of signal is eliminated. → Low pass filter
- As a 3KHz component drops 6dB than a 1.5KHz component because of the low pass filter, compensation is therefore done. → High frequency compensation
- The output level is set to the micro level. → Attenuation
- DC component is cut. → DC decoupling



C1, C2: DC decuppling
Output level: 3mV rms
Output impeadance: APROX 600Ω

4-2. Read circuit



The read signal amplifier circuit consists of the same type as that of the CE-150. The circuitry is contained inside the gate array in the case of the CE-1600P.

4-3. Remote circuit

For the relay (AG8229 or G5AK-287P) is a two-coil latching type, A ON (or OFF) pulse must be given to the activate (or deactive) the relay through the driver of the gate array, in order to turn the relay active. (See Fig.8.)
The width of pulse must be more than 5 milliseconds than that mentioned in the relay specification. With the CE-1600P, it is set to about 10 milliseconds.

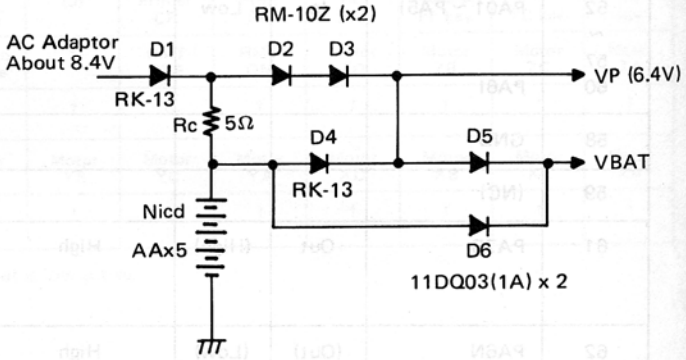
The following signal formats are used for the cassette interfacing signals.

Write . . . . . PWM method (1600 method)
Read . . . . . PWM method (1600 method) and 1500 method

5. Power supply circuit

5-1. Power supply

VP, VBAT, and battery recharge circuits



D1: For prevention of reverse current to the rechargeable battery to the adaptor.
To achieve efficient recharging of the battery, a Schottky barrier type diode RK-13 (1.7A) is used.

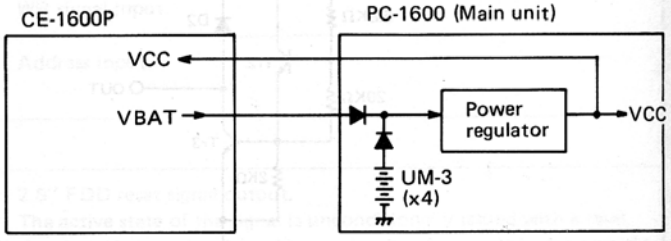
D2, D3: These diodes are used to drop the voltage from the printer to less than printer driving voltage (7.15V max.).

D4: For prevention of reverse current from VP to the rechargeable battery, when the adaptor is being used.

D5: For prevention of reverse current from VBAT (PC-1600) to VP (printer).
The diode is a Schottky battery type for avoiding battery exhaustion when the adaptor is used.

D6: To avoid exhaustion of the battery in the main unit when the rechargeable battery is used, D6 is used to bypass D4 and D5.
To meet the printer drive voltage (5.0V, min.), the rechargeable battery low voltage is set to 5.65V limit (1.13V per battery).

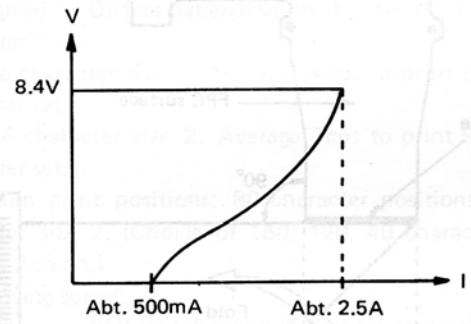
After the main unit battery is ORed with the VBAT supply from the CE-1600P, VCC is regulated to 4.7V before supplied to the CE-1600P. (See the figure below.)
When the main unit power is turned off, VCC is not supplied.



5-2. AC adaptor (EA-160)

The following is a brief specification.

- Primary side input rating
  100VAC, 50/60Hz, 20VA (Japan use)
- Secondary side output
  Rated voltage: 8.4VDC
  Rated current: 1A
  Peak current: 2A
  Overcurrent protection: About 2.5A
  (Output short protection)



  Regulator type: Chopper
- Size of case and weight
  67.2 mm (W) x 115.2 mm (D) x 53.5 mm (H) excluding the stand of 1 mm high.
  695 g

6. Service precautions

- All components must be closely installed on the board.
- Observe the following torque in tightening the tapping screw. Too much force may damage such as cabinet. For the type of the screw to be used, refer to Parts Guide.

Screw location number (See Parts Guide).	Tightening torque (kg-cm)
A	2.0 kg • cm
B	2.5 kg • cm
C	3.0 kg • cm

Marking in Parts Guide
The symbol (A to C) is attached to the lower right side of the parts number.
Ex: 4A

- Consumption current

VP = 6V

		Consumption current	Note
PC-1600		Max. 50mA	RS-232C not in operation
Printer	Gate array (LR38045)	Max. 3.25mA	at 1.3MHz
	ROM (SC27C256)	Max. 3.20mA	At 400KHz
	Driver (LB1247)	Max. 100mA	
	When 45° dotted line is printed	Max. 803mA	
	When print ASCII character	Max. 638mA	
	When "555 ...." printed	Max. 605mA	
	When the carriage is is returning	Max. 242mA	
	45° dotted line	Max. 959.45mA	
	ASCII character	Max. 794.45mA	
	"555....."	Max. 761.45mA	

NOTE: Printing character standard "2"

- Maximum printing time
  (i) When printing 45° dotted line: 28 minutes
  (ii) When printing ASCII character: 34 minutes
  (iii) When printing "555....": 35 minutes

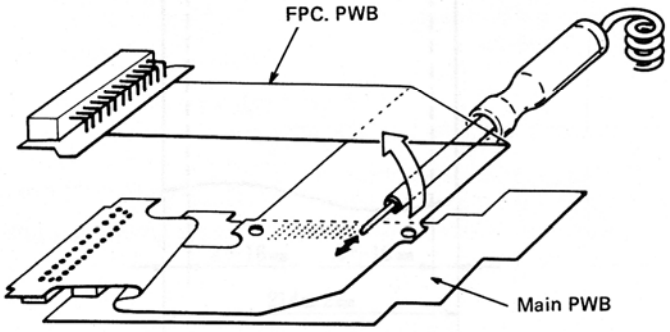
* Rechargeable battery capacity: 500mAH (at full charge)

** Maximum printable characters: About 10,000 characters (at print speed of 5 CPS)

*** Maximum printable lines: About 240 lines (at the print speed of 5 CPS, with one second considered for a carriage return after printing 40 character positions on a line)

6-1. Removal of the FPC PWB

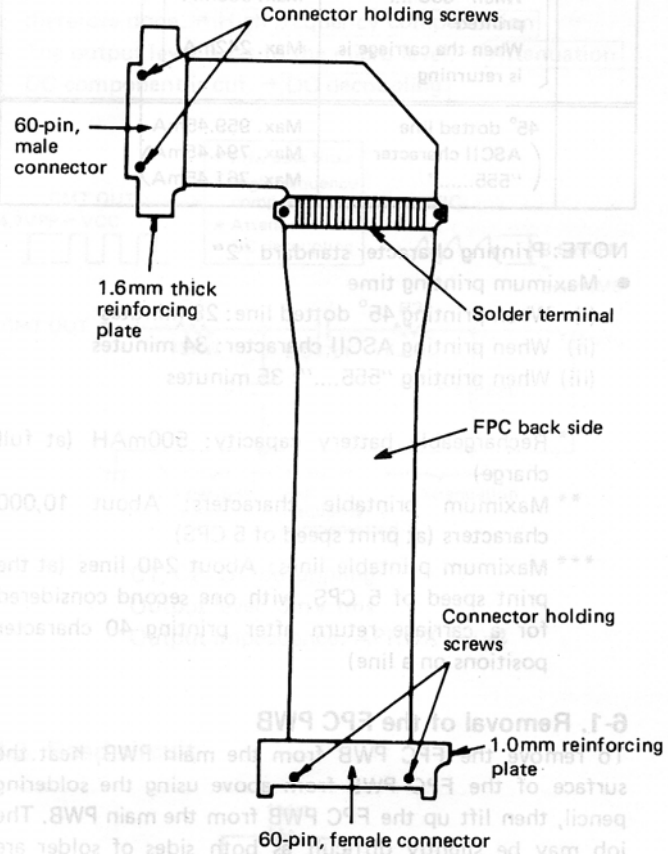
To remove the FPC PWB from the main PWB, heat the surface of the FPC PWB from above using the soldering pencil, then lift up the FPC PWB from the main PWB. The job may be slightly difficult as both sides of solder are secured with the double tack tape.



6-2. Soldering FPC and connector

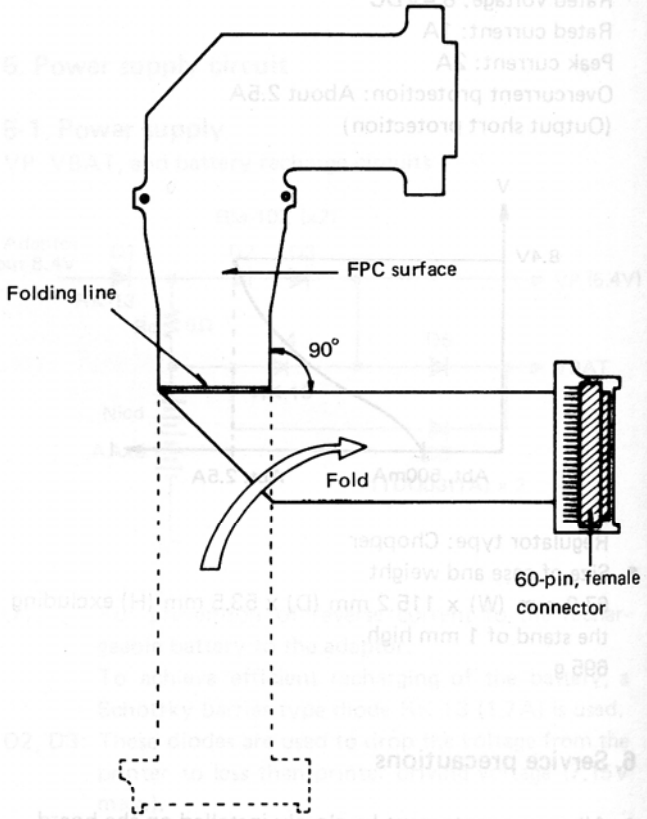
Insert the 60-pin male connector (GCNCM1295CC6J) and the 60-pin female connector (QCNCW1293CCZZ) to the FPC PWB (QPWBM1009ECZZ) and secure them with screws. Then, solder the connectors with the soldering pencil, with care for line intervention by solder. Connect the male connector to the 1.6 mm thick reinforcing plate and the female connector to the 1.0 mm thick reinforcing plate.

Next, align the longer connector with the shorter connector, then cut it to the same length as the shorter connector.

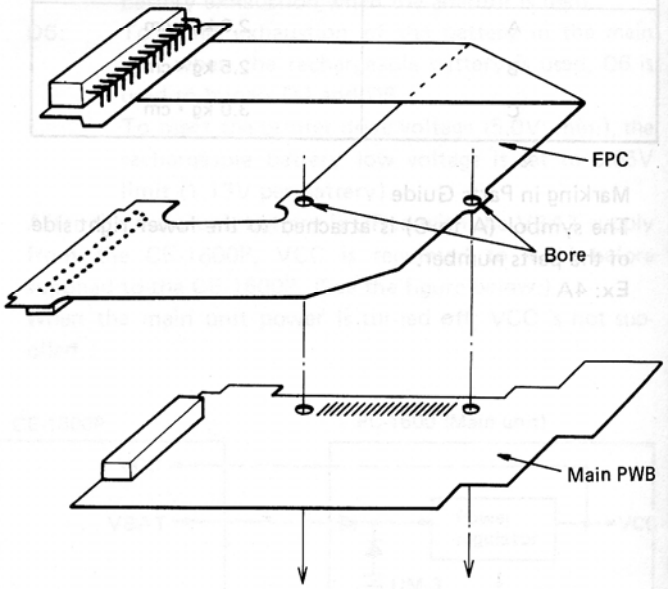


6-3. Soldering the FPC PWB (DUNTK1060ECZZ) and main PWB

① Fold the FPC in reference to the line shown on the surface of the FPC (the side the solder terminal is not on).



② Evenly solder the solder terminal area on the surface of the main PWB and clean the area with alcohol. Match the bores in the FPC with the bores in the main PWB, then temporarily fix using the double tack tape of the FPC.



③ Heat the FPC PWB from above using the soldering pencil to solder it. (Solder temperature: 260°C)

7. Printer block (PTMPG3308A)

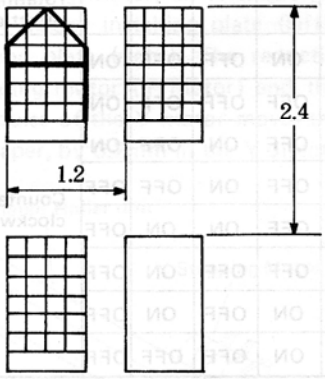
As specifications given in this section are for servicing of the printer mechanism, they may differ from those given in Page 00 which take precedence over the specifications in this section.

7-1. Specifications of the PTMPG3308A

Model name: PTMPG3308A
Recording media: Four-color rotary ball point pen recorded
Mechanisum: Drum type X-Y plotter
Print speed: Differs depending on the size of the printed character.
For the character size 1: Average 14cps to print 96 ASCII character set.
For the character size 2: Average 7cps to print 96 ASCII character set.
Maximum print positions: 80 character positions for the character size 2. (Choice of 160, 120, 40 character positions and so on.)
Pen moving speed:
X axis . . . . . 650 steps/second (1-2 phase excitation)
325 steps/second (2-2 phase excitation)
Y axis . . . . . 650 steps/second

Pen moving distance:
X axis . . . . . 0.1mm (0.2mm during initialization)
Y axis 0.1mm
Pen plotting speed:
65mm/second (X and Y axis)
92mm/second (45 degrees)
Character size: Character size differs depending on the character form.

5 x 7 matrix



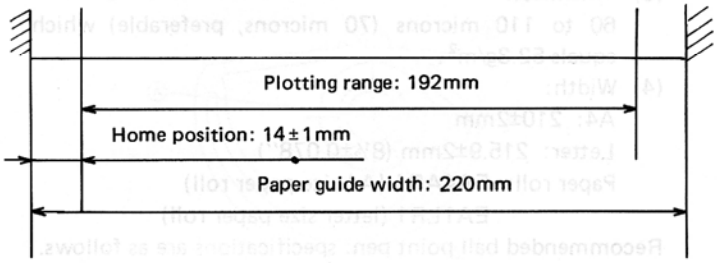
- Character dimensions:
0.8mm x 1.2mm (minimum)
(1.05mm x 1.45mm in the case of 0.25mm line width)
- Print pitch: 1.2mm±10%
- Paper feed pitch: 2.4mm±10 %

Character size	1	2	3	4	5	6	7	8	9
Characters/Line	160	80	53	40	32	26	22	20	17
Character height (mm)	1.2	2.4	3.6	4.8	6.0	7.2	8.4	9.6	10.8
Character width (mm)	0.8	1.6	2.4	3.2	4.0	4.8	5.6	6.4	7.2

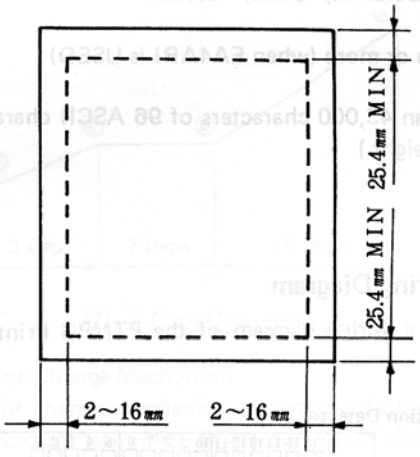
Plotting range

1) Plotting direction
Horizontal pen movement to the right is along the +X direction and to the left is along the −X direction Paper feed is along the Y direction, having the paper fed derection along the −Y direction.

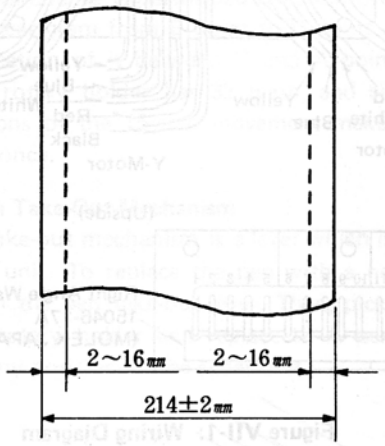
2) Plotting range
(1) X-axis
192mm, 1920 steps



(2) Y-axis
i) A4 size and letter sizes



ii) Paper roll (recommended type)



(A variation of 2 to 16mm may occur depending on how the paper is set.)

Recording paper

The following paper specifications are recommended to meet the write and paper feed requirements of the ball point pen.

1) Cut sheet

(1) Kind:
Plain paper

(2) Paper quality:
Must be a high-quality paper whose surface smoothness is more than 25 seconds without oil material on surface.

(3) Thickness:
60 to 110 microns (70 microns, preferable) which equals 52.3g/m^2.

(4) Width:
A4: 210±2mm
Letter: 215.9±2mm (8½±0.078")
Paper roll: EA4AR1 (A4 size paper roll)
EA1LR1 (letter size paper roll)

Recommended ball point pen: specifications are as follows.

(1) Kind:
Water based

(2) Size:
ϕ5 x 23.3mm, +0mm, −0.1mm

(3) Life:
250m or more (when EA4ARI is USED)

(More than 43,000 characters of 96 ASCII character set of 2.4mm height.)

3. A Wiring Diagram

Below is a wiring diagram of the PTMPG Printer Circuit Board.

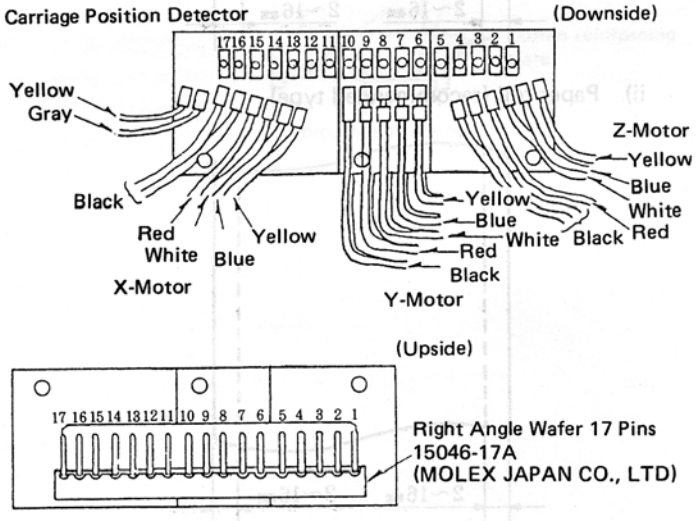


Figure VII-1: Wiring Diagram

4. Circuit Diagram

Below is a circuit diagram of the PTMPG Printer Circuit Board.

Name	Phase	Color	No.	Circuit
Carriage Position Detector	B	Gray	17	
	A	Yellow	16	
X-motor (Carriage Movement)	COM	Black	15	
	D	Red	14	
	C	White	13	
	B	Blue	12	
	A	Yellow	11	
Y-motor (Paper-Feeding)	COM	Black	10	
	D	Red	9	
	C	White	8	
	B	Blue	7	
	A	Yellow	6	
Z-motor (Pen-Up/ Down & Color-Change)	COM	Black	5	
	D	Red	4	
	C	White	3	
	B	Blue	2	
	A	Yellow	1	

Figure VII-2: Circuit Diagram

Drive pulse train

X-axis and Y-axis drive motors (1-2 phase excitation)

Step No.	A	B	C	D	Motor shaft rotating direction	Moving direction	
						X-axis	Y-axis
1	ON	OFF	OFF	ON	Counter-clockwise	+ Clock-wise	+ Reverse feed
2	OFF	OFF	OFF	ON			
3	OFF	ON	OFF	ON			
4	OFF	ON	OFF	OFF			
5	OFF	ON	ON	OFF			
6	OFF	OFF	ON	OFF			
7	ON	OFF	ON	OFF			
8	ON	OFF	OFF	OFF			

The X-axis motor operates under the 2-2 phase excitation mode during initialization.

Z-axis drive motor (2-2 phase excitation)

Step No.	A	B	C	D	Motor shaft rotating direction	Moving direction
1	ON	OFF	OFF	ON	Counterclock-wise	+ Pen down
2	OFF	ON	OFF	ON		
3	OFF	ON	ON	OFF		
4	ON	OFF	ON	OFF		

7-2. Physical Characteristics of the printer

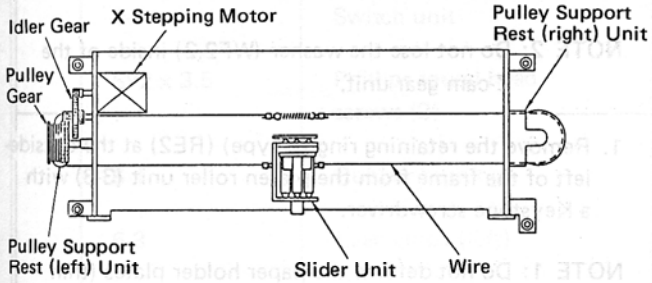
The PTMPG printer is composed of five parts: a frame unit, an X-direction drive unit, a Y-direction drive unit, a pen drive mechanism & color-change mechanism, and a pen take-out mechanism. Each part is described below.

1. The Frame unit

The frame unit consists of a right side-plate, a left side-plate, support plate and paper guide. The lower end of the frame is used for mounting.

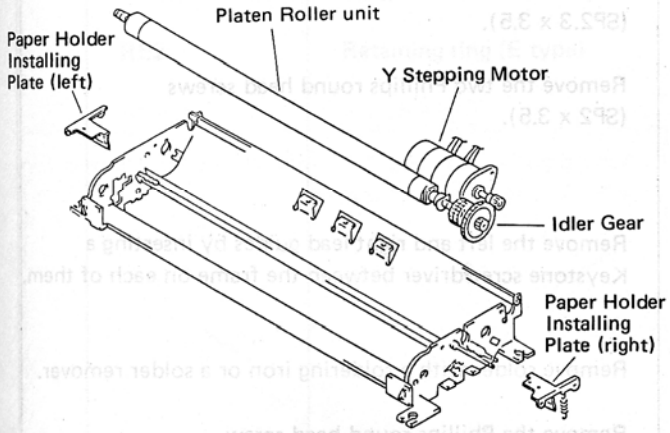
2. The X-Direction Drive unit

The X-direction drive unit consists of an X stepping motor, an idler gear, a pulley gear, a pulley support rest (left) unit, a pulley support rest (right) unit, a slider unit, and a wire. The gear reduction ratio of the stepping motor and pulley gear is 1:13.9. A single pulse of the stepping motor (18 degrees/360) moves the slider unit or pen by 0.2mm in the X direction. Power transmission from the pulley gear to the slider unit is made by the wire, which is tensioned by a coil spring.



3. The Y-Direction Drive unit

The Y-direction drive unit is the paper-feed mechanism. It consists of a Y stepping motor, an idler gear, a platen roller unit, a paper holder installing plate (left), and a paper holder installing plate (right). The reduction ratio between the Y stepping motor (Y motor) and the platen gear is 1:7.88. One pulse of the Y motor moves the platen roller, or recording paper, by 0.2mm in the Y direction.



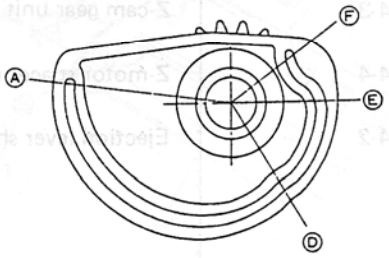
4. The Pen Drive Mechanism & Color-Change Mechanism

This part consists of two main blocks: the pen drive mechanism and the color-change mechanism, each of which is described below.

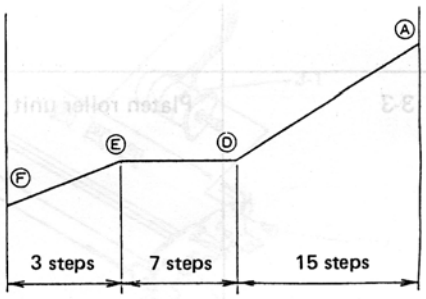
1) The Pen Drive Mechanism

The pen drive mechanism consists of a Z-motor unit, a Z-cam gear, an ejection lever shaft unit, a roller lever and a ball point pen.

The pen's up/down movements are performed by the rotation of the cam gear, whose motive power is transferred to the ejection lever through a pin. Considering the E point below as an origin, the pen comes down when the cam gear rotates three (3) steps along Z (+) direction, and the pen comes up when the cam gear rotates three (3) steps from the pen-down position along Z (−) direction.



(1) View of the Z-Cam Gear



(2) Z-Cam Gear steps

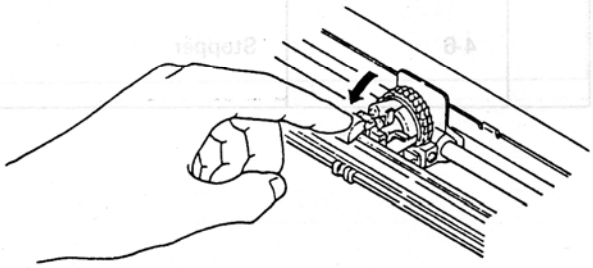
2) The Color-Change Mechanism

The color change mechanism is composed of a Z-motor unit, a Z-cam gear unit, an ejection lever shaft unit, a rotary holder which is in the slider unit, and a color-change lever.

The color-change is performed by the movement of the Z-cam gear gram from E point to D point and then the reciprocation of it between D and A points. The gear of the rotary holder has 32 teeth, and eight (8) reciprocations of the 15-step movement make for a color change once.

5. The Pen Take-Out Mechanism

The pen take-out mechanism is a lever which is attached to the slider unit. To replace the pen with a new one, first press down the pen take-out lever. Then, pick up the pen from the rotary holder and replace it. A pen can be repalced at any position on the slider unit.



7-3. Disassembly and Assembly

This section gives step-by-step instructions for taking apart and a ssembling the PTMPG printer. It also contains the adjustment methods of each part, and wiring and circuit diagrams for the circuit board on the printer.

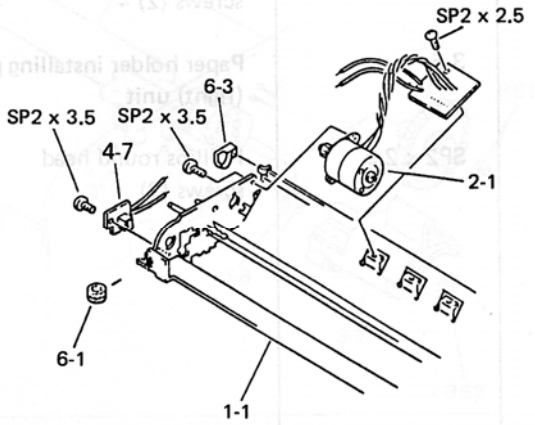
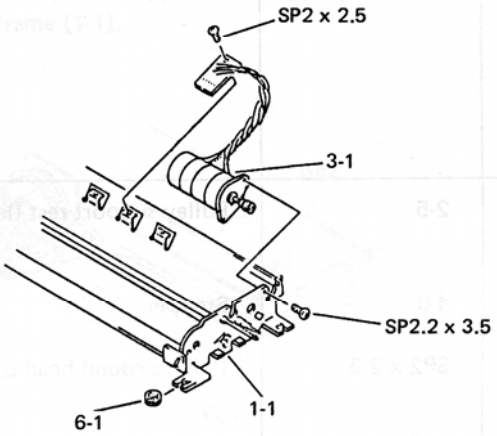
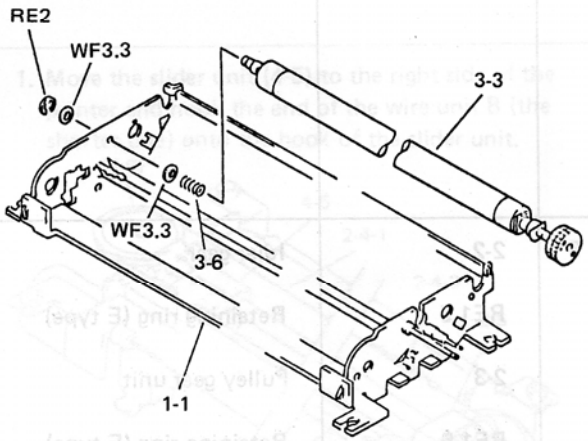
1. Disassembly

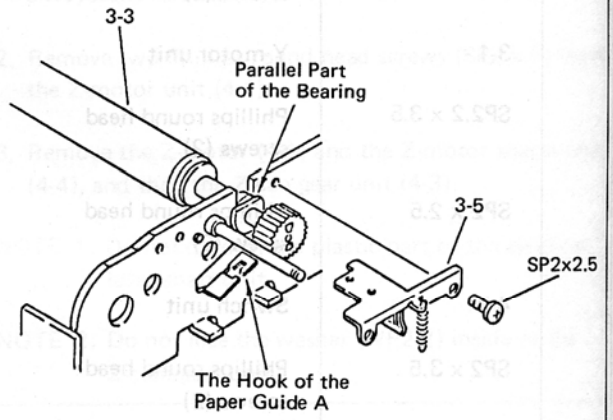
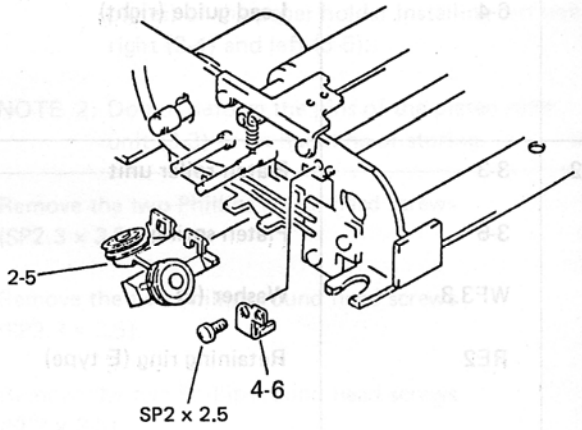
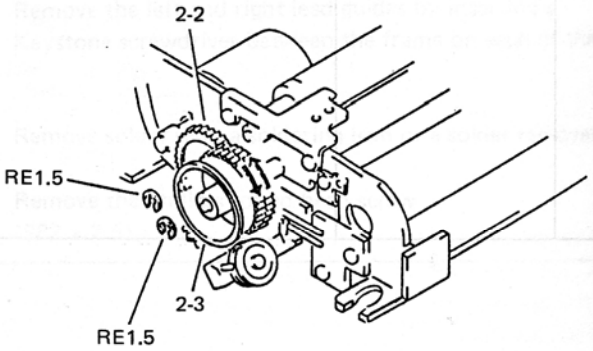
To take apart the PTMPG printer, remove the components from the frame in the order shown below. Where necessary, an explanation is supplied in the right-hand column.

Step	Part No.	Component	Explanation
1	4-1	Z-motor unit	1. Remove the retaining ring (E type) (RE1.5) and the plain washer (WF2.2) from the Z-cam gear unit with a Keystone screwdriver.
	4-3	Z-cam gear unit	
	4-4	Z-motor spacer unit	2. Remove two Phillips round head screws (SP2 x 5) from the Z-motor unit (4-1).
	4-2	Ejection lever shaft unit	3. Remove the Z-motor (4-1) and the Z-motor spacer unit (4-4), and then the Z-can gear unit (4-3).
			NOTE 1: Do not deform the plastic part of the ejection lever shaft unit.
			NOTE 2: Do not lose the washer (WF2.2) inside of the Z-cam gear unit.
2	3-3	Platen roller unit	1. Remove the retaining ring (E type) (RE2) at the outside-left of the frame from the platen roller unit (3-3) with a Keystone screwdriver.
			NOTE 1: Do not deform the paper holder plates (thin plates) of the paper holder installing rest units, right (3-4) and left (3-5).
			NOTE 2: Do not deform the pins of the platen roller unit (3-3) when handling or storing.
3	2-1	X-motor unit	Remove the two Phillips round head screws (SP2.3 x 3.5).
	3-1	Y-motor unit	Remove the two Phillips round head screws (SP2.3 x 3.5).
	4-7	Switch unit	Remove the two Phillips round head screws (SP2 x 3.5).
	6-1	Rubber bushing	
	6-3	Lead guide (left)	Remove the left and right lead guides by inserting a Keystone screwdriver between the frame on each of them.
	6-4	Lead guide (right)	
	6-2	Wafer assembly	Remove solder with a soldering iron or a solder remover.
	4-6	Stopper	Remove the Phillips round head screw (SP2 x 2.5).

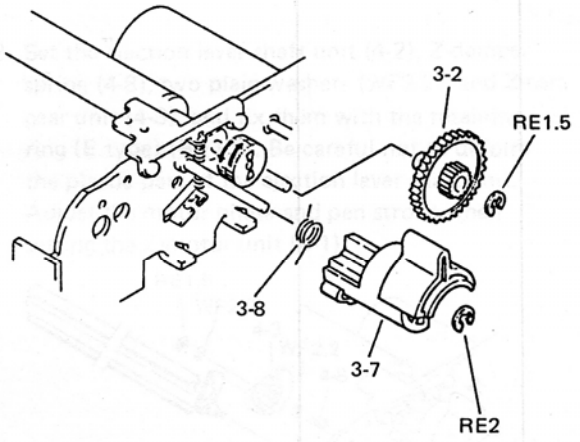
2. Assembly

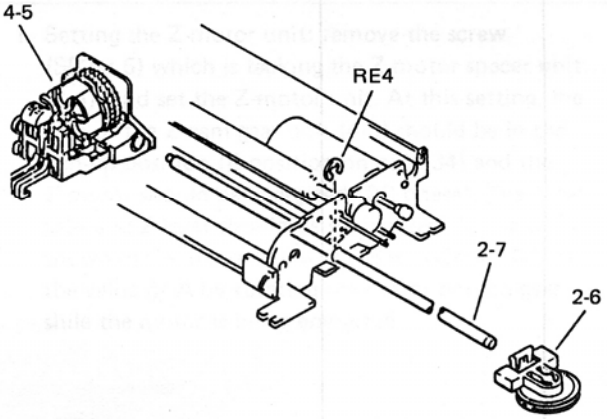
To assemble the PTMPG printer, follow the assembling order of the instructions shown below.
Before assembling the Z-motor unit, adjust for pen-stroke and motor phase.

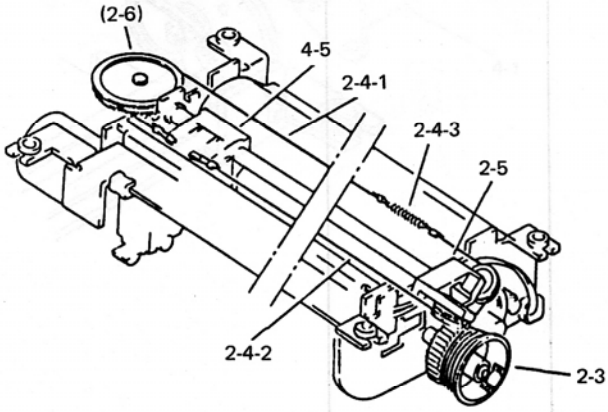
Step	Part No.	Component	Explanation
1	2-1	X-motor unit	
	SP2 x 3.5	Phillips round head screws (2)	
	SP2 x 2.5	Phillips round head screws (2)	
	3-1	Y-motor unit	
	SP2.2 x 3.5	Phillips round head screws (2)	
	SP2 x 2.5	Phillips round head screw (2)	
	4-7	Switch unit	
	SP2 x 3.5	Phillips round head screws (2)	
	6-1	Rubber bushing	
	6-3	Lead guide (left)	
	6-4	Lead guide (right)	
2	3-3	Platen roller unit	
	3-6	Platen spring	
	WF3.3	Washer (2)	
	RE2	Retaining ring (E type)	

Step	Part No.	Component	Explanation
3	3-4	Paper holder installing plate (left) unit	The paper holder installing plate (right) unit serves as a fixer of the bearing or the platen roller unit (3-3), too. Set it with the parallel part of the bearing up.
	SP2 x 2.5	Phillips round head screws (2)	
	3-5	Paper holder installing plate (right) unit	The screw-tightening torque is 2.5 kg/cm.
	SP2 x 2.5	Phillips round head screws (2)	After tightening the screws, hook the paper holder spring onto the hook of the paper guide A of the frame (1-1).
			
4	2-5	Pulley support rest (left) unit	Press the pulley support rest (left) unit (2-5) into the frame (1-1).
	4-6	Stopper	The screw-tightening torque is 2.5 kg/cm.
	SP2 x 2.5	Phillips round head screw	
5	2-2	Idler gear	Set the pulley gear unit (2-3) to shift into double-gear with the cog. (Mark the cog first.)
	RE1.5	Retaining ring (E type)	
	2-3	Pulley gear unit	
	RE1.5	Retaining ring (E type)	

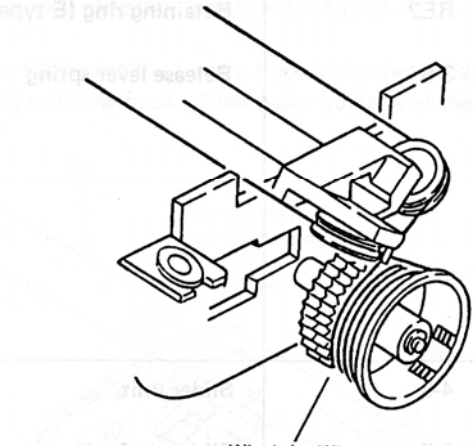
Step	Part No.	Component	Explanation
6	3-2	Idler gear	Shift the double-gear (platen gear) of the roller unit (3-3) with the cog, and set the idler gear (3-2). (Mark the cog first.)
	RE1.5	Retaining ring (E type)	
	3-7	Release lever	
	RE2	Retaining ring (E type)	
	3-8	Release lever spring	
7	4-5	Slider unit	Press the pulley support rest (right) unit (2-6) into the frame (1-1).
	2-7	Slider shaft	
	RE4	Retaining ring (E type)	
	2-6	Pulley support rest (right) unit	
8	2-4-1	Wire unit A	1. Move the slider unit (4-5) to the right side of the printer and hook the end of the wire unit B (the shorter one) onto the hook of the slider unit.
	2-4-2	Wire unit B	
	2-4-3	Wire spring	

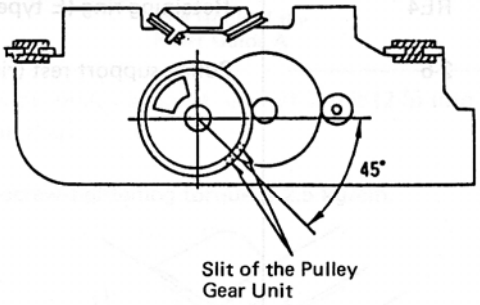




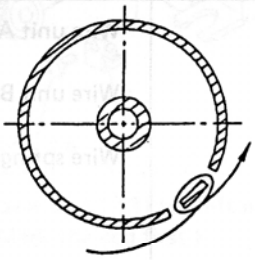


Step	Part No.	Component	Explanation
8			2. Wind the wire around the pulley of the pulley support rest (right) unit (2-6). After winding the wire unit A (the longer one) around the pulley support rest (left) unit (2-5) as shown in step1, wind it four (4) times around the pulley gear unit (2-3). The position of the second figure is shown be lox.

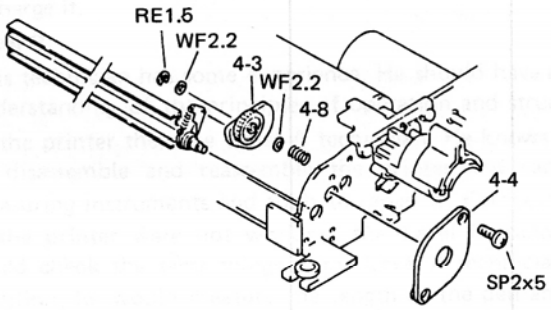
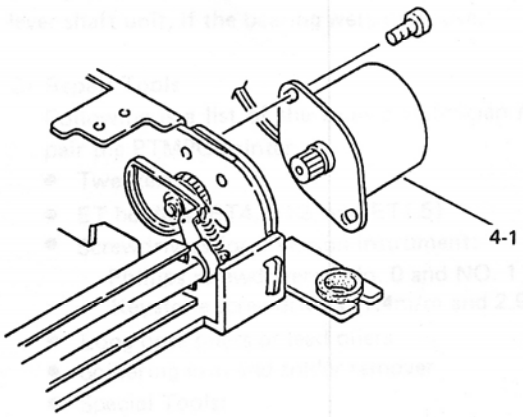


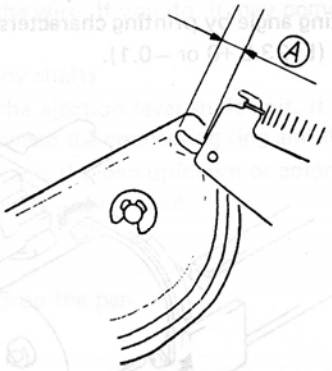


3. Pass the wire through the slit of the pulley gear unit and wind it around the other pulley of the pulley support rest (left) unit (2-5). Then, hook it onto the left-side hook of the slider unit.

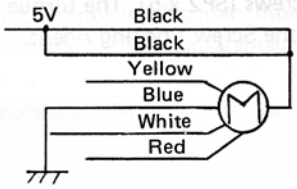


4. Test to confirm the condition of the wire unit by checking whether the slider unit can be moved smoothing front side to side by hand.

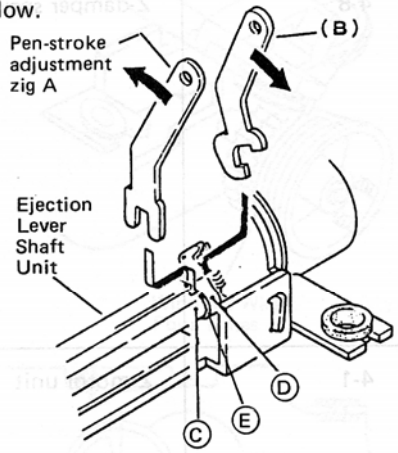
Step	Part No.	Component	Explanation
9	4-2	Ejection lever shaft unit	1. Temporarily fix the Z-motor spacer unit (4-4) onto the frame with a Phillips round head screw (SP2 x 5). 2. Set the ejection lever shaft unit (4-2), Z-damper spring (4-8), two plain washers (WF2.2), and Z-cam gear unit (4-3), and fix them with the retaining ring (E type) (RE1.5). Be careful not to deform the plastic part of the ejection lever shaft unit. Adjust the motor phase and pen stroke when setting the Z-motor unit (4-1). 
	4-3	Z-cam gear unit	
	WF2.2	Plain washers (2)	
	4-4	Z-motor spacer unit	
	SP2 x 5	Phillips round head screw	
	4-8	Z-damper spring	
10	4-1	Z-motor unit	1. Setting the Z-motor unit: remove the screw (SP2 x 5) which is tacking the Z-motor spacer unit (4-4), and set the Z-motor unit. At this setting, the cam of the Z-cam gear unit (4-3) should be in the pen-up position (E position on page 34) and the Z-motor should be energized (BC phase). The Z-cam gear and Z-lever should be so engaged that value A shown in the figure below is 0.8 to 1.0mm. Adjust the value of A by rotating the motor ponion gear shile the motor is being energized. 



BC Phase Energizing

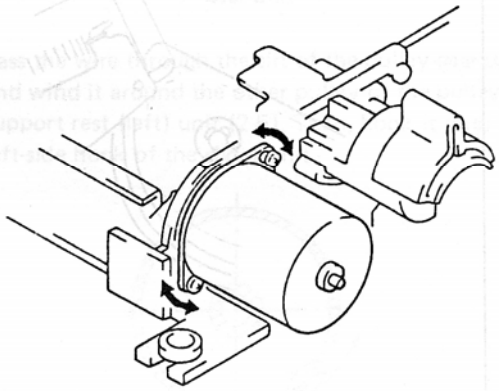


Step	Part No.	Component	Explanation
10			2. Adjustment of the pen stroke: using the pen stroke adjustment jigs, A and B, rotate the depressed part of the connecting ring of the ejection lever shaft unit. Using a standard pen (L = 23.3 +0 or −0.1), the pen stroke (the gap between a pen tip and a platen) must be 0.6 to 0.7mm at pen-up position (the horizontal part of the Z-cam gear in Figure V1-4). To make the pen stroke smaller, move the pen stroke adjustment jigs of A and B in each direction indicated by the arrows in the figure below.



After adjustment, apply the Screw Locking Agent to position E in the above figure.

3. Adjustment of the Z-motor phase: adjust the motor-setting angle by printing characters with a standard pen (L=23.3 +0 or −0.1).



4. Tightening the screw: tighten the Phillips reoud head screws (SP2 x 5). The torque is 2.5 kg/cm. Apply the Screw Locking Agent.

7-4. Maintenance and Repair

This section gives general instructions for handling the PTMPG printer. Directions for maintenance and repair are also included.

1. Handling the PTMPG Printer

The PTMPG printer should be handled carefully and gently. If you follow the instructions given below, your PTMPG printer should give years of service. The sections below give tips for proper handling of the printer.

1) Holding the Printer

Hold the front and rear of the printer (marked with ⇩), as shown in Figure IX-1 below. The printer could malfunction if it is held on the sides (marked with ⇨). Do not squeeze the ejection lever shaft unit when you hold the printer.

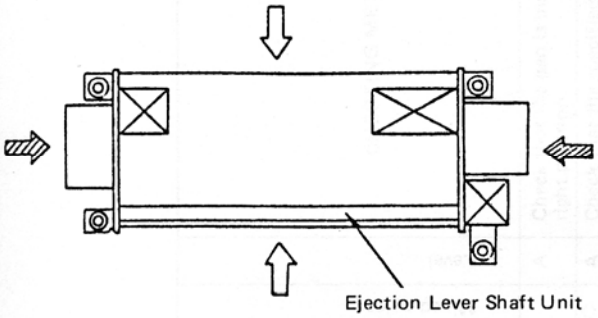


Figure IX-1

2) Parts That Should Not Be Touched

- Do not touch the slider unit, except to take out the pen.
- Do not touch the wire. If you do, it may come out of the pulley.
- Do not touch any shafts.
- Do not touch the ejection lever shaft unit. If you do, the relation between the connecting ring and the shaft will be shifted, and the pen-up/down or color-change functions may not be performed.

3) Handling the Pen

Be careful not to drop the pen.

2. Maintenance

The PTMPG printer should be cleaned every three months, or after using 5 rolls of paper, whichever comes first.

Remove paper debris, dirt, and dust by suction (using a vacuum cleaner). If necessary, apply alcohol or petroleum benzine to remove dirt. Do not use lacquer thinner, trichloroethylene or ketone solvents. They can damage the plastic parts.

Grease the printer, if necessary. Apply the grease to specified parts only.

3. Repairing the PTMPG Printer

This section covers instructions for repairing the PTMPG printer, including descriptions of the levels of skill a technician must have to perform different types of repair jobs, a list of the tools a technician will need, and a comprehensive Repair Guide that shows remedies for problems that might occur.

1) The Repair Technician

There are three levels of repair technicians: A, B, and C. Each level is based on the level of knowledge about and the skills required in repairing the PTMPG printer.

Level A:

This technician has little experience. He has general knowledge of the principles of operation and structure of the printer. He does not require extensive experience or skill. For example, suppose the printer does not print. The Level A technician would first check to see if the solenoid were energizing. If necessary, he would replace it or repair the driving circuit. If the solenoid were enegizing properly, he would check the battery voltage and, if neccessary, recharge it.

Level B:

This technician has some experience. He should have more understanding of the principles of operation and structure of the printer than the Level A technician. He knows how to disassemble and reassemble the printer and can use measuring instruments and tools to repair it. For example, if the printer were not working, the Level B technician could check the same things as the Level A technician. In addition, he would measure the length of the pen and replace it if it were too short. He could check the actuator, or look for a broken spring in the solenoid, and replace the unit if necessary. He could also replace the rotary holder for the pen if it were defective.

Level C:

This technician is highly experienced. He should have detailed knowledge of the principles of operation and structure of the printer, a high level of capability in printer disassembly and reassembly, experience with measuring instruments and tools, and the ability to repair all parts of the printer. The Level C technician would perform all of the tasks of Levels A and B. In addition, he would replace the ejection lever if it were bent, and replace the ejection lever shaft unit, if the bearing were defective.

2) Repair Tools

Following is a list of the tools a technician needs to repair the PTMPG printer.

- Tweezers
- ET holders (ET4, ET2, and ET1.5)
- Screwdrivers for precision instrument:
  Phillips screwdrivers: No. 0 and NO. 1
  Keystone screwdrivers: 1.4m/m and 2.9m/m
- Long nose pliers or lead pliers
- Soldering iron and solder remover
- Special Tools:
  a set of pen-stroke adjustment jigs:
  Adjustment jig A 00P72-0012/// FG
  Adjustment jig B 00P72-0013/// FG
  Thickness gauge

3) The Repair Guide

A Repair Guide is shown in the following pages. It is divided into five columns for ease of reference. Descriptions of the five columns are shown on the next page:

"Problem": This column contains the problem you have identified. Look here first.

"Cause": This column describes the causes of a problem under the specified conditions.

"Level": This is the level of expertise of the repair technician.

"Checking Method": This column describes the points in the printer to be checked to locate the malfunctioning part.

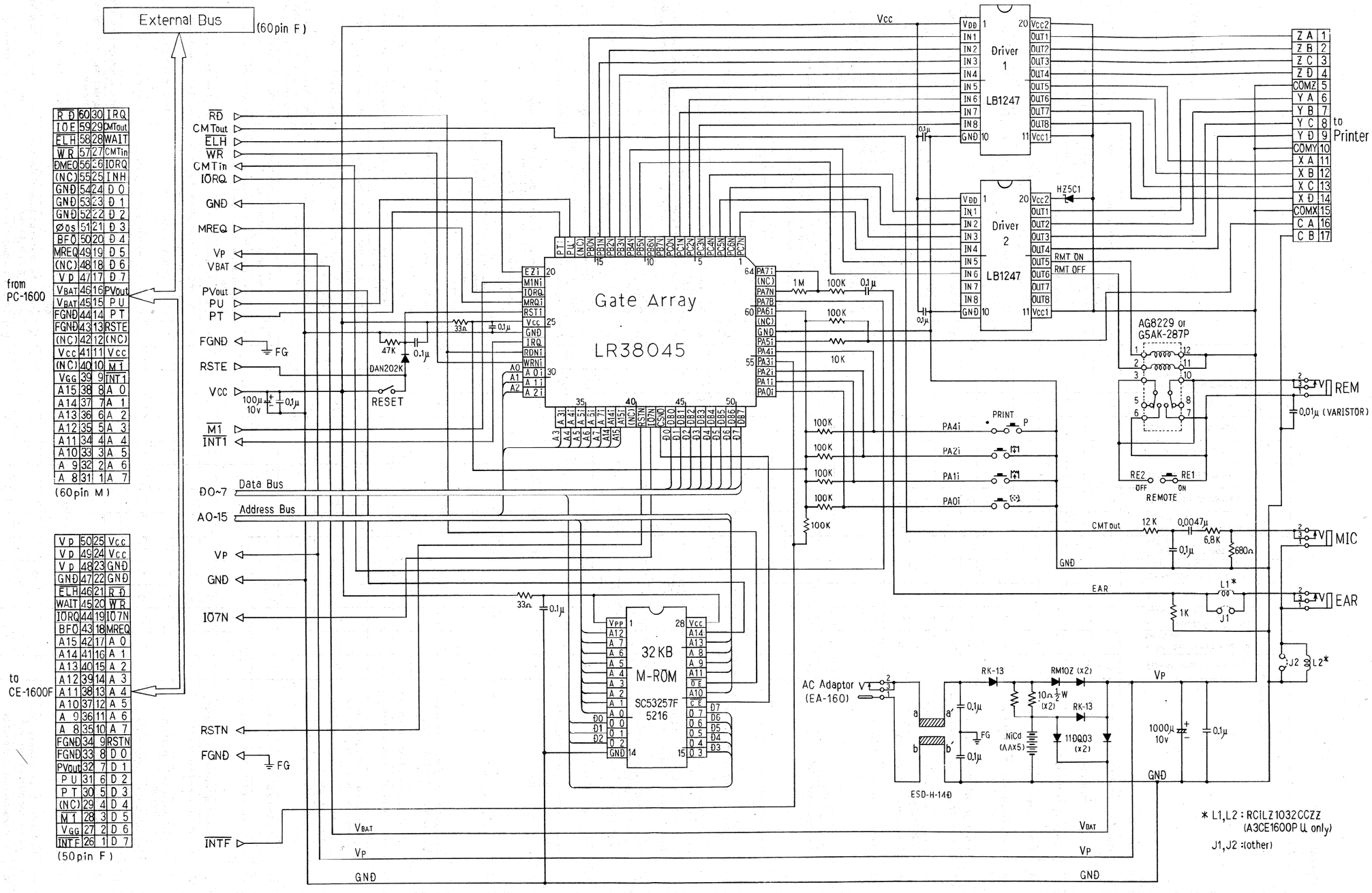
"Repairing Method": This column contains instructions for repairing the printer.

Look up "Problem" on Table X-1 first to identify your problem and find its "Cause." The reference numbers of each "Cause" correspond with the ones of the "Checking Method" and "Repairing Method" on Table X-2 in the following pages.

Repair Guide

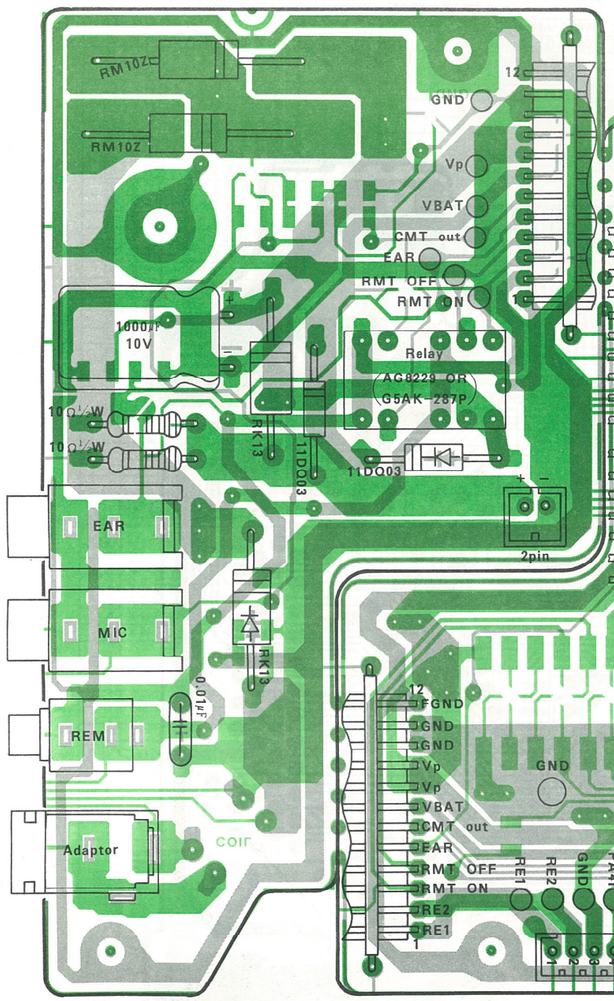
REF. NO.	CAUSE \ PROBLEM	The printer does not draw	A horizontal line cannot be drawn	Small movement in the horizontal direction	Paper is not fed	Small movement in the vertical direction	The pen does not go down	Draw with one stroke of the pen	Misshapen characters	Blurred characters	Broken characters	Stains on the margin	Color can not be changed	Unanticipated pen color appears	Mixed colors	Level	CHECKING METHOD	REPAIRING METHOD
1	Improper installation of the pen	○							○				○	○		A	Check that the pen is installed in the right position.	Attach the pen correctly.
2	Using an unspecified pen	○					○	○		○	○	○	○	○	○	A	Check that the specified pen (length: 23.3 +0 or −0.1 mm) is attached.	Attach the specified pen.
3	The pen is out of ink	○								○						A	Check whether the pen is out of ink by handwriting.	Attach a new pen.
4	The lead wire of the Y-motor is cut		○													B	Check that the proper current flows into each phase of the X-motor.	Replace the X-motor unit.
5	Malfunction of the X-motor unit		○	○					○							B	Remove the X idler gear and check the motor gear for any unusual load by turning it slowly.	Replace the X-motor unit.
6	Broken or deformed X idler gear		○	○					○							A	Check the X idler gear.	Replace the X idler gear.
7	Broken or deformed pulley gear unit		○	○					○							B	Check the pulley gear.	Replace the pulley gear unit.
8	Foreign materials in the teeth of X-drive gear		○	○					○							A	Check for foregin materials	Remove foregin materials
9	The battery voltage drops	○	○	○	○	○	○	○	○				○	○		B	Check the battery voltage make sure the voltage is more than 5.15V	1) Charge or replace the battery
10	Unsmooth sliding of slider unit		○	○					○							B	Remove the wire and make sure that the slider unit can be moved smoothly from side to side by hand.	1) Remove foreign materials. 2) Replace the slider unit. 3) Clean the shaft and add a lubricant.
11	The wire is cut	○	○													B	Check whether the wire is cut.	Replace the wire unit.
12	The wire is taken off	○	○	○												B	Check if the wires have come off from the pulley gear and from the pulleys of the pulley support rest right and left units.	Rewire correctly.
13	Worn wire spring or stretched wire								○							B	Check whether the wire is stretched, and that the wire spring is worn.	Replace the wire unit.
14	Deformed ejection lever shaft unit			○			○	○					○	○		C		Replace the ejection lever shaft unit.
15	Rollers of the pulley support rests (R & L) do not rotate			○												B	Remove the wire and check that the pulleys rotate smoothly.	Replace the pulley support rest unit.
16	Slider unit is in contact with the paper guide or its rollers		○	○												B	Check for contact by moving the slider from side to side when the release lever is ON.	Replace the slider unit. If the roller spring of the paper guide is deformed, replace the spring.
17	Improper relation between the two gears of the pulley gear unit			○					○							A	Check the relative position of the two gears of the pulley gear.	Put the two gears together correctly.
18	The lead wire of the Z-motor is cut	○	○				○	○					○	○		C	Check that the proper current flows into each phase of the motor.	Replace the Z-motor unit.
19	Deformed Z-cam gear	○	○				○	○					○	○		C	Check for the deformation of the Z-cam gear, especially the grooves on it.	Replace the Z-cam gear.
20	Foreign materials in the teeth of the Z-drive gear	○	○				○	○					○	○		A	Check for foreign materials.	Remove foreign materials.
21	Bigger pen stroke						○			○	○					C	Measure the pen stroke of the specified pen (length: 23.3 +0 or −0.1 mm) to make sure that the gap is 0.7 to 0.8 mm.	Adjust the pen stroke correctly.
22	Smaller pen stroke						○	○				○				C	Measure the pen stroke of the specified pen (length: 23.3 +0 or −0.1 mm) to make sure that the gap is 0.7 to 0.8 mm.	Adjust the pen stroke correctly.
23	Removed or deformed color-change lever spring of the slider unit												○	○		B	Check whether the color-change lever spring is either removed or deformed.	Replace the color-change lever spring.
24	Defective switch of the switch unit													○		B		Replace the switch unit.
25	The lead wire of the switch unit is cut													○		B	Check that the proper current flows into the switch.	Replace the switch unit.
26	Deformation or breakage of the penreturn spring of the slider unit						○	○	○	○	○		○	○		B	Check for deformation or breakage of the pen-return spring.	Replace the slider unit.
27	Deformed or broken detent plate of the slider unit								○				○	○		B	Check for deformation or breakage of the detent plate.	Replace the slider unit.
28	Removed holder ring of the slider unit												○	○		A	Check if the holder ring is removed from the rotary holder.	Set the holder ring in the rotary holder properly. Replace the holder ring, if its click is broken.
29	The lead wire of the Y-motor is cut				○											B	Check that the proper current flows into each phase of the motor.	Replace the Y-motor unit.
30	Mulfunction of the Y-motor unit					○										B	Remove the Y-idler gear and check the motor gear for any unsual load by turning	Replace the Y-motor unit.
31	Deformed or broken Y-idler gear				○	○										A	Check the Y-idler gear.	Replace the Y-idler gear.
32	Platen roller does not rotate				○	○			○							B	Remove the Y-idler gear and check the rotation of the platen roller.	Replace the platen roller.
33	Foreign materials in the teeth of the Y-drive gear				○	○										A	Check for foreign materials.	Remove foreign materials.
34	The rollers of the paper guide do not rotate smoothly				○	○										A	Check that the rollers of the paper guide rotate smoothly.	Replace the printer mechanism.
35	Foreign materials in the paper guide				○	○										A	Check for foreign materials.	Remove foreign materials.
36	Deformed paper-holder installing plates (L & R)				○	○	○									A	Check if the paper-holder installing plate unit is deformed and touches the slider unit or the platen roller.	Replace the paper-holder installing plate unit.
37	Unspecified paper is used				○	○	○		○	○						A	Check the paper size, thickness, and quality.	Use specified paper.
38	Improper relation betweem the two gears of the platen roller unit					○			○							A	Check the relative position of the two gears of the platen gear.	Put the two gears together correctly.
39	Worn bearing part of the rubber roller					○			○							A	Check for a bigger backlash of the R shaft and the bearing.	Replace the platen roller unit.

8. CIRCUIT DIAGRAM

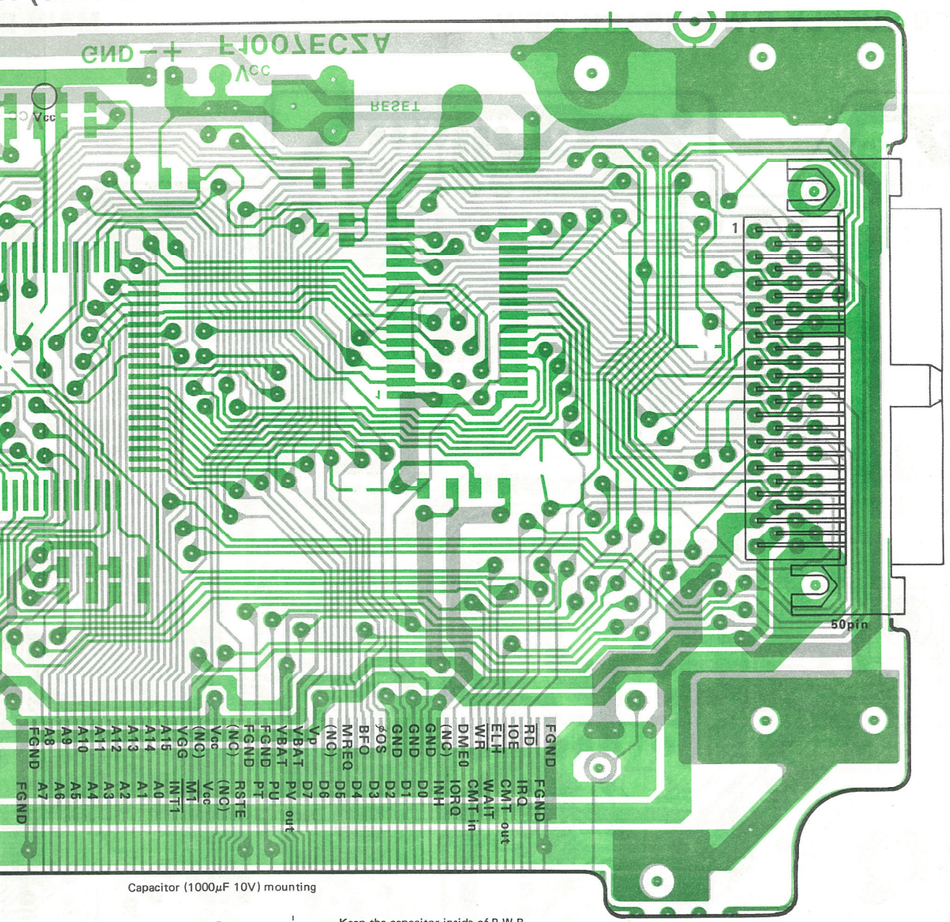


9. PARTS & SIGNAL POSITION

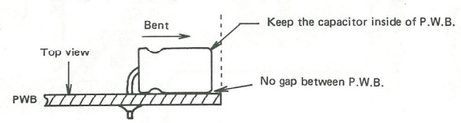
POWER SUPPLY P.W.B. (FRONT VIEW)



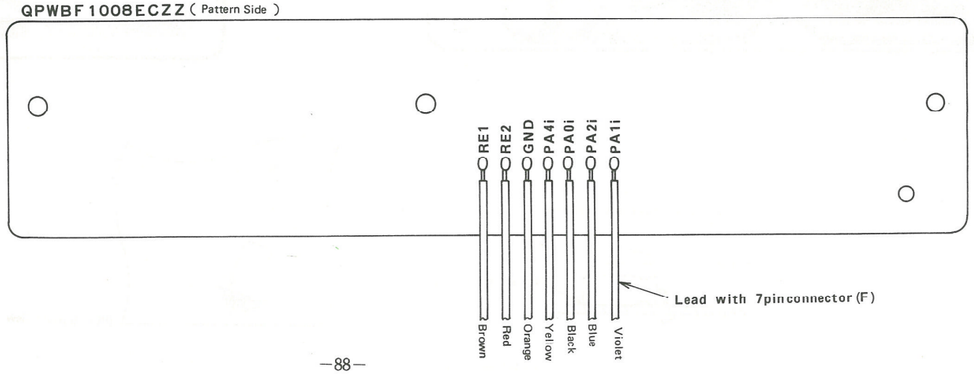
MAIN P.W.B. (CONNECTOR-SIDE)



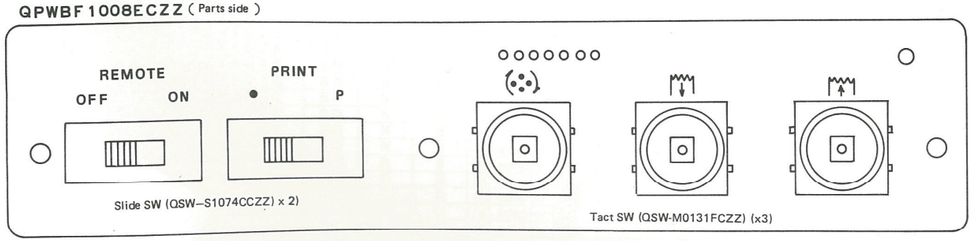
Capacitor (1000μF 10V) mounting



QPWBF1008ECZZ (Pattern Side)

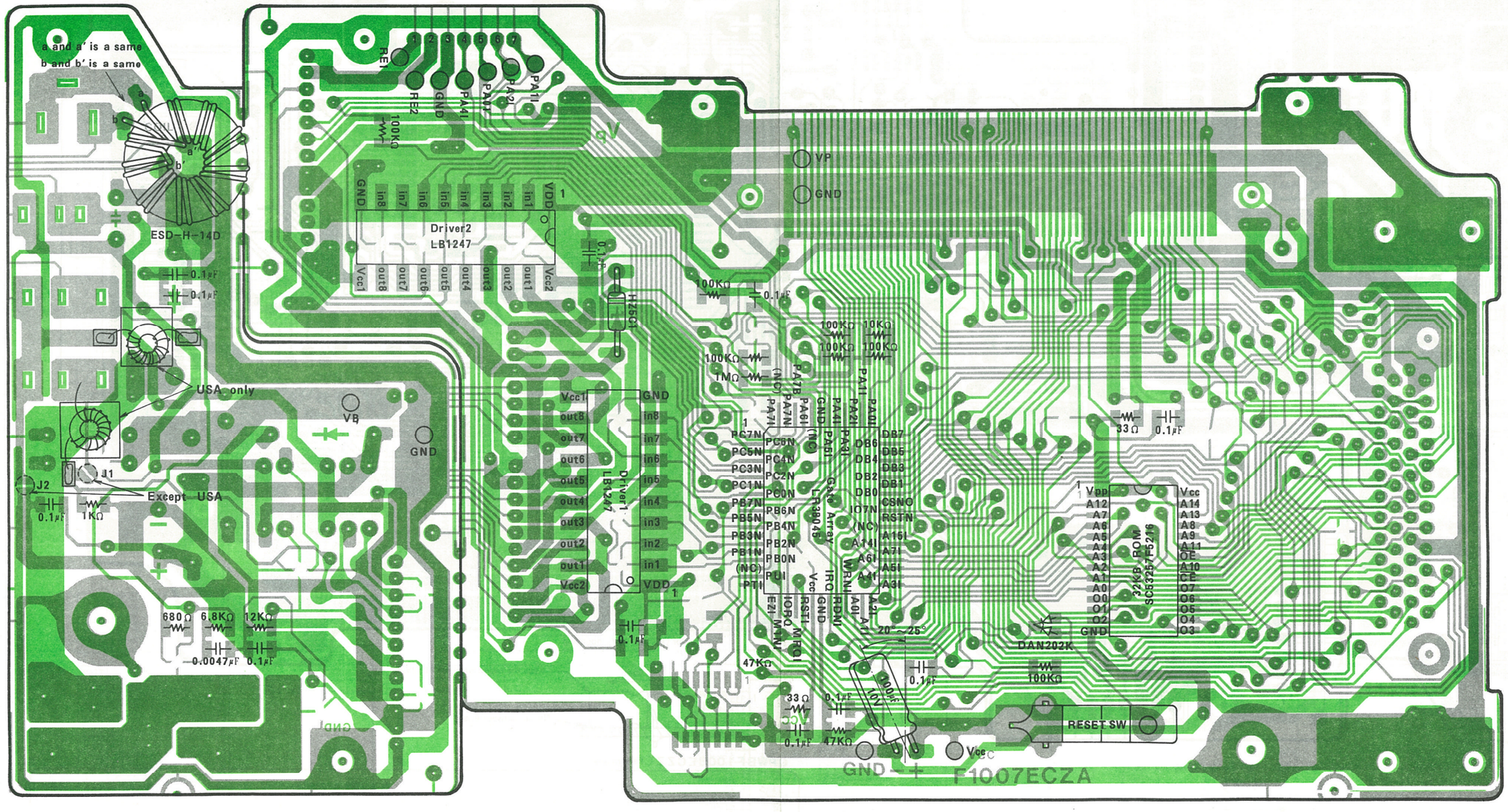


QPWBF1008ECZZ (Parts side)

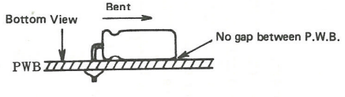


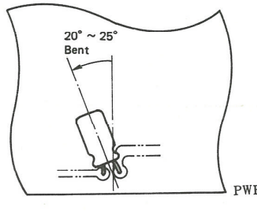
POWER SUPPLY P.W.B. (BACK VIEW)

MAIN P.W.B. (LSI SIDE)



Capacitor (100μF 10V) mounting





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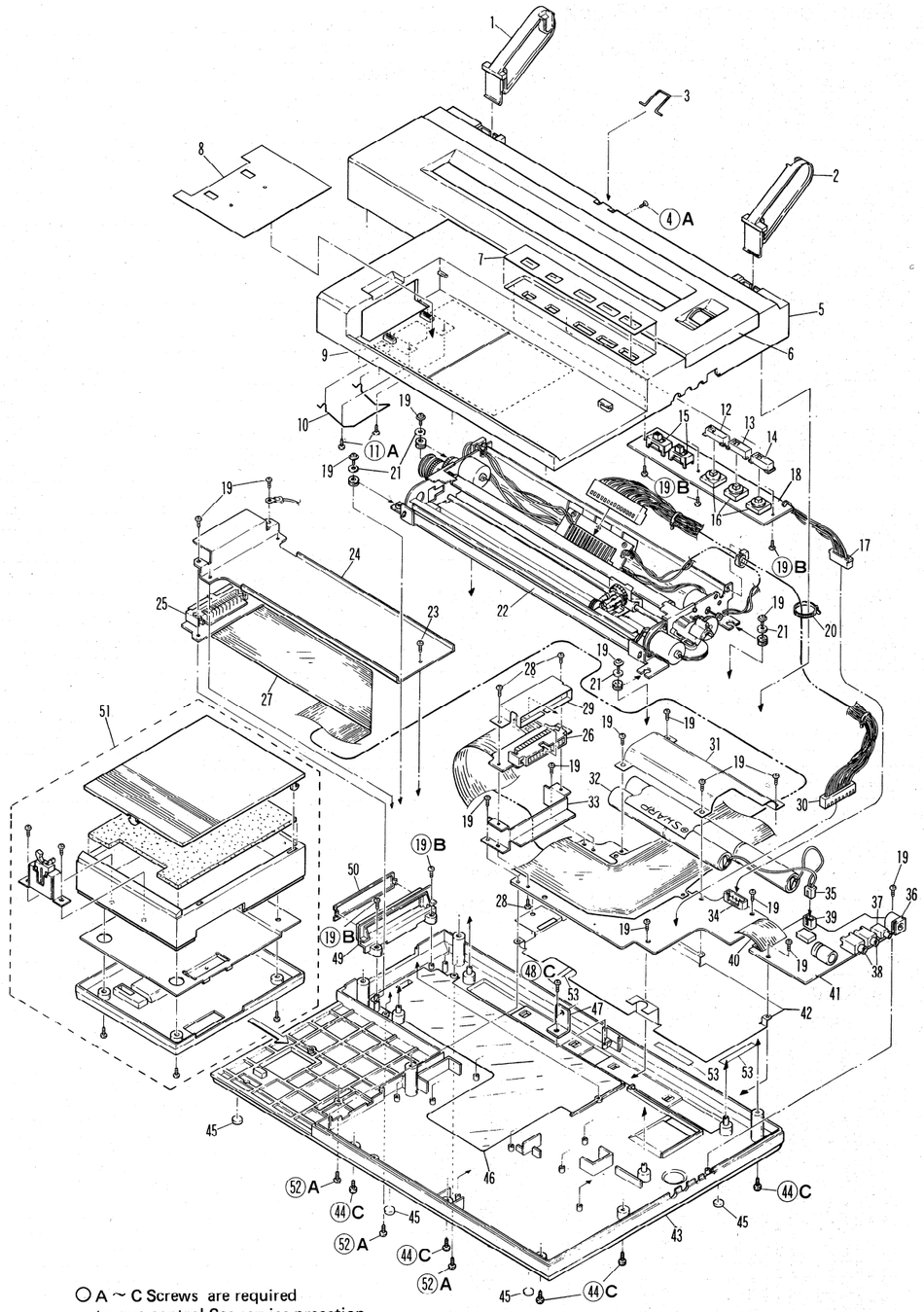
10. PARTS LIST & GUIDE

1 Exteriors

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	LHLDZ1002FECZZ	AB	N	D	Paper holder (Left)
2	LHLDZ1003ECZZ	AB	N	D	Paper holder (Right)
3	LPiN−1001ECZZ	AB	N	C	Pin
4	XBSSM20P06000	AA		C	Screw (2×6)
5	GCABB1010ECZZ	AT	N	D	Top cabinet
6	CCOVA1003EC01	AL	N	D	Printer cover
7	HDECA1012ECZZ	AE	N	D	Switch panel
8	HDECA1011ECZZ	AF	N	D	Dec.panel
9	PTPEH1006ECZZ	AD	N	C	Static tape B
10	QTANZ1003ECZZ	AC	N	C	Static terminal
11	LX−BZ1155CCZZ	AA		C	Screw (2×8)
12	JKNBZ1952CCSA	AM	N	C	Color change key (18PCS/set)
13	JKNBZ1952CCSB	AM	N	C	Reverse paper feed key (18PCS/set)
14	JKNBZ1952CCSC	AM	N	C	Paper feed key (18PCS/set)
15	QSW−S1074CCZZ	AE		B	Slide switch
16	QSW−M0131FCZZ	AC		B	Key switch
17	QCNCW1007EC0G	AE	N	C	Connector (7pin)
18	DUNTK1057ECZZ	AV	N	E	Switch PWB unit (This includes №15~17)
19	XUBSD20P06000	AA		C	Screw (2×6)
20	LBNDJ2003SCZZ	AA		C	Cable clamp
21	LX−WZ1010ECZZ	AA	N	C	Washer
22	DUNT−1042ECZZ	BW	N	E	Printer unit (PTMPG3308A)
23	XUBSD20P04000	AA		C	Screw (2×4)
24	GiTAZ1002ECZZ	AF	N	C	FPC fixing plate
25	QCNCW1293CCZZ	AY		C	Connector (60pin)
26	QCNCM1295CC6J	AV		C	Connector (60pin)
27	DUNTK1060ECZZ	BN	N	E	FPC PWB unit (This includes№25,26)
28	XBBSD20P06000	AA		C	Screw (2×6)
29	PSLDC1008ECZZ	AE	N	C	Connector shield plate
30	QCNCW1006EC1G	AN	N	C	Connector (17pin)
31	LANGK1006ECZZ	AD	N	C	Battery fixing angle
32	UBATN1003ECZZ	BA	N	A	Battery (NI−CD AA3×5)
33	LANGK1005ECZZ	AG	N	C	Connector fixing angle
34	QCNCM5016SC0G	AB		C	Connector (7pin)
35	QCNCW1008EC0B	AB	N	B	Connector (2pin)
36	QJAKC1003CCZZ	AD		B	Jack for AC adaptor
37	QJAKC1016CCZZ	AC		C	Jack socket (for Remote)
38	QJAKC1013CCZZ	AC		B	Jack for MIC
39	QCNCM1338CC0B	AA		B	Connector (2pin)
40	QCNW−1011ECZZ	AC	N	C	FPC
41	DUNTK1059ECZA	BT	N	E	Main·Power supply PWB unit (USA only) (This includes №28,33,34,36~40)
	DUNTK1059ECZZ	BT	N	E	Main·Power supply PWB unit (Other countries) (This includes №28,33,34,36~40)
42	PSLDC1007ECZZ	AF	N	C	Shield plate
43	GCABA1009ECZZ	AQ	N	D	Bottom cabinet
44	XUBSD26P08000	AA		C	Screw (2.6×8)
45	GLEGP1009CCZZ	AA		C	Rubber foot
46	PTPEH1005ECZZ	AF	N	C	Static tape A
47	LANGK1007ECZZ	AC	N	C	Fixing angle
48	XUBSD26P06000	AA		C	Screw (2.6×6)
49	GWAKP1041CCZZ	AF		C	Connector frame
50	GFTAA1267CCSA	AB	N	D	Connector cover
51	DUNT−1058ECZZ	AW	N	E	Dummy case unit
52	XBBSM20P06000	AA		C	Screw (2×6)
53	PTPEH1084CCZZ	AA		C	Tape (47×5)

2 Main·Power supply PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	LANGK1005ECZZ	AG	N	C	Connector fixing angle
2	RCiLZ1032CCZZ	AD		C	Coil (USA only)
3	PSHEZ1144CCZZ	AA		C	Sheet (USA only)
4	QCNTM1051CCZZ	AB		C	Reset terminal
5	QCNCM1338CC0B	AA		B	Connector (2pin)
6	QCNCM5016SC0G	AB		C	Connector (7pin)
7	QCNCW1004EC5J	AS	N	C	Connector (50pin)
8	QCNW−1011ECZZ	AC	N	C	FPC
9	QJAKC1003CCZZ	AD		B	Jack for AC adaptor
10	QJAKC1013CCZZ	AC		B	Jack (for MIC)
11	QJAKC1016CCZZ	AC		C	Jack socket (for Remote)
12	QLUGE1005CCZZ	AA		C	Lug terminal
13	RC−CZ1021CCZZ	AB		C	Capacitor (0.1μF)
14	RC−CZ1039CCZZ	AB		C	Capacitor (4700pF)
15	RC−CZ1077CCZZ	AC		C	Capacitor (16WV 10000pF)
16	RFiLN1008CCZZ	AH		C	Filter (ESD−H−14B)
17	RRLYZ2400QCZZ	AP		B	Relay
18	VCEAGU1AW107M	AB		C	Capacitor (10WV 100μF)



○ A ~ C Screws are required torque control See service precation on section 6. (page 69)

2 Main・Power supply PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
19	VCEAGU1AW108M	AC		C	Capacitor (10WV 1000μF)
20	VHDDAN202K/−1	AB		B	Diode (DAN202K)
21	VHDRK13////−1	AF	N	B	Diode (RK13)
22	VHDRM10Z////−1	AC	N	B	Diode (RM10Z)
23	VHD11DQ03//−1	AE		B	Diode (11DQ03)
24	VHEHZ5C1////−1	AB		B	Zener diode (HZ5C1)
25	VHiLB1247///−1	AM		B	IC (LB1247)
26	VHiLR38045/−1	AQ	N	B	IC (LR38045)
27	VHi53257F5216	AU	N	B	IC(53257F5216)
28	VRS−TP2BD473J	AA		C	Resistor (1/4W 47KΩ ±5%)
29	VRD−RB2HY100J	AA	N	C	Resistor (1/2W 10Ω ±5%)
30	VRS−TP2BD102J	AA		C	Resistor (1/8W 1KΩ ±5%)
31	VRS−TP2BD103J	AA		C	Resistor (1/8W 10KΩ ±5%)
32	VRS−TP2BD104J	AA		C	Resistor (1/8W 100KΩ ±5%)
33	VRS−TP2BD105J	AA		C	Resistor (1/8W 1.0MΩ ±5%)
34	VRS−TP2BD123J	AA		C	Resistor (1/8W 12KΩ ±5%)
35	VRS−TP2BD330J	AA		C	Resistor (1/8W 33Ω ±5%)
36	VRS−TP2BD681J	AA		C	Resistor (1/8W 680Ω ±5%)
37	VRS−TP2BD682J	AA		C	Resistor (1/8W 6.8KΩ ±5%)
38	XBBSD20P06000	AA		C	Screw (2×6)
39	XBBSD20P08000	AA		C	Screw (2×8)
40	XNESD20−16000	AA		C	Nut (M2)
	(Unit)				
901	DUNTK1059ECZA	BT	N	E	Main・Power supply PWB unit (USA only)
	DUNTK1059ECZZ	BT	N	E	Main・Power supply PWB unit (Other countries)

3 FPC PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	QCNCW1293CCZZ	AY		C	Connector (60pin)
2	QCNCM1295CC6J	AV		C	Connector (60pin)
3	XBBSD20P08000	AA		C	Screw (2×8)
4	XBBSD20P10000	AA		C	Screw (2×10)
5	XNESD20−16000	AA		C	Nut (M2)
	(Unit)				
901	DUNTK1060ECZZ	BN	N	E	FPC PWB unit

4 Switch PWB unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	QCNCW1007EC0G	AE	N	C	Connector (7pin)
2	QSW−M0131FCZZ	AC		B	Key switch
3	QSW−S1074CCZZ	AE		B	Slide switch
	(Unit)				
901	DUNTK1057ECZZ	AV	N	E	Switch PWB unit

5 Packing material & Accessories

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	LHLDZ1002ECZZ	AB	N	D	Paper holder(Left)
2	LHLDZ1003ECZZ	AB	N	D	Paper holder(Right)
3	NSFTZ1002ECZZ	AL	N	C	Paper shaft (USA only)
	NSFTZ1001ECZZ	AL	N	C	Paper shaft (A4 size)(Other countries)
4	QPLGJ1022CCZZ	AQ		C	Cassette cable plug
⚠ 5	RADPA1004ECZZ	BM	N	B	AC adaptor (USA)
⚠	RADPA1004ECZA	BM	N	B	AC adaptor (MV)
⚠	RADPA1004ECZB	BN	N	B	AC adaptor (MB)
⚠	RADPA1004ECZC	BN	N	B	AC adaptor (MA)
⚠	RADPA1004ECZD	BN	N	B	AC adaptor (SH)
⚠	RADPA1004ECZE	BN	N	B	AC adaptor (SE)
⚠	RADPA1004ECZF	BN	N	B	AC adaptor (SB)
⚠	RADPA1004ECZG	BN	N	B	AC adaptor (SC)
⚠	RADPA1004ECZH	BN	N	B	AC adaptor (SK)
⚠	RADPA1004ECZi	BN	N	B	AC adaptor (SN)
⚠	RADPA1004ECZJ	BN	N	B	AC adaptor (SM)
⚠	RADPA1004ECZK	BM	N	B	AC adaptor (SJ)
⚠	RADPA1004ECZL	BN	N	B	AC adaptor (SD)
6	TiNSE1032ECZZ	AR	N	D	Instruction book (USA only)

5 Packing material & Accessories

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
6	TiNSM1033ECZZ	BC	N	D	Instruction book (E,F,G,S,I)
7	UBAGZ1001ECZZ	AZ	N	D	Hard case
8	SPAKA0050ECZZ	AK	N	D	Packing cushion
9	SPAKC0094ECZZ	AK	N	D	Packing case
10	SPAKA0178ECZZ	AD	N	D	Packing cushion for accessories
11	SPAKA0179ECZZ	AC	N	D	Sheet for paper
12	SPAKA146ACCZZ	AB		D	Packing cushion
13	PCAPH1013CCZZ	AD		C	60pin Connector cap
14	TCAUK1191CCZZ	AA		D	Caution card
15	GLEGP1030CCZZ	AB		C	Rubber spacer for hard case (1.6T)

6 Printer unit

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION	
1	00PDG275//////	BA		C	Frame unit	(1−1)
2	00P01G0557////	AR		C	Paper guide B	(1−1−1)
3	00PDG249//////	BB		C	X motor unit	(2−1)
4	00P07G0247////	AL		C	Idler gear	(2−2)
5	00PDG214//////	AN		C	Pulley gear unit	(2−3)
6	00P17G0029////	AR		C	Wire unit(A)	(2−4−1)
7	00P17G0028////	AR		C	Wire unit(B)	(2−4−2)
8	00P19G0367///	AD		C	Wire spring	(2−4−3)
9	00PDG218//////	AR		C	Roller fixing base unit(left)	(2−5)
10	00PDG219//////	AN		C	Roller fixing base unit(right)	(2−6)
11	00P10G0493////	AR		C	Slider shaft	(2−7)
12	00P30−0309−00	AC		C	Screw	(SP2×3.5)
13	00P30−0307−00	AA		C	Screw	(SP2×2.5)
14	00P27−0002−19	AA		C	E type ring	(RE1.5)
15	00P27−0006−19	AB		C	E type ring	(RE4)
16	00PDG250//////	BK		B	Y motor unit	(3−1)
17	00PDG265//////	BB		C	Platen roller unit	(3−3)
18	00P07G247//////	AL		C	Idler gear	(3−2)
19	00PDG216//////	AR		C	Paper hold plate unit(left)	(3−4)
20	00P19G0369////	AD		C	Paper holder spring	(3−5−1)
21	00PDG217//////	AR		C	Platen spring	(3−5)
22	00P19G0369////	AD		C	Paper holder spring	(3−5−1)
23	00P19G0365////	AC		C	Platen spring	(3−6)
24	00P12G0204−11	AE		C	Release lever(gray)	(3−7)
25	00P19G0391////	AD		C	Release lever spring	(3−8)
27	00P30−0409−00	AA		C	Screw	(SP2.3×3.5)
29	00P27−0003−19	AA		C	E type ring	(RE2)
30	00P23G0056−01	AC		C	Washer	(WF3.3)
31	00PDG224//////	BG		C	Z motor unit	(4−1)
32	00PDG260//////	AZ		C	Ejection lever shaft unit	(4−2)
36	00P19G0370////	AD		C	Z lever spring	(4−2−4)
38	00PDG237//////	AK		C	Z cam gear unit	(4−3)
39	00PDG223//////	AQ		C	Z motor spacer	(4−4)
40	00PDG262//////	AW		C	Slider (II) unit	(4−5)
41	00PDG240//////	AN		C	Rotary holder unit	(4−5−1)
42	00PDG206//////	AU		C	Slider (I) unit	(4−5−2)
43	00P01G0703////	AN		C	Card guide	(4−5−3)
44	00P01G0549////	AG		C	Shaft hold plate	(4−5−4)
45	00P34L0309−00	AC		C	Screw	(4−5−5)
46	00P19G0372////	AD		C	Color−change lever spring	(4−5−6)
47	00P13G0554////	AC		C	Detent plate	(4−5−7)
48	00P13G0547−04	AN		C	Holder ring	(4−5−8)
49	00P13G0549////	AF		C	Stopper	(4−6)
50	00PDG276//////	AP		B	Switch unit	(4−7)
51	00P62−0010////	AG		B	Carriage position detector switch	(4−7−1)
52	00P19G0381////	AC		C	Z damper spring	(4−8)
53	00P30−0312−00	AC		C	Screw	(SP2×5)
57	00P23−0057////	AA		C	Waher	(WF2.2)
58	00P23G0049////	AE		C	Rubber bushing	(6−1)
59	00P63G4021////	AP		C	Wafer assembly	(6−2)
60	00P11G0179////	AD		C	Lead guide(Left)	(6−3)
61	00P11G0178////	AD		C	Lead guide(Right)	(6−4)
62	00P68G1179////	AK		C	Earth wire	(6−5)
63	00P24−0008−00	AC		C	Waher	(WF2.8)
64	00P30−4C08−00	AB		C	Screw	(SP2.6×3)
101	00PDG259//////	AY		C	Ejection lever unit	(4−2−1)
102	00P13G0559////	AD		C	Connecting ring	(4−2−2)
103	00PDG236//////	AK		C	Z cam lever unit	(4−2−3)
104	00P72−0012////	AT		C	Pen−stroke adjustment jig A	(7−1)
105	00P72−0013////	AT		C	Pen−stroke adjustment jig B	(7−2)
	(Unit)					
901	DUNT−1042ECZZ	BW	N	E	Printer unit (PTMPG3308A)	

Index

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
【C】				
CCOVA1003EC01	1- 6	AL	N	D
【D】				
DUNT-1042ECZZ	1- 22	BW	N	E
//	6- 901	BW	N	E
DUNT-1058ECZZ	1- 51	AW	N	E
DUNTK1057ECZZ	1- 18	AV	N	E
//	4- 901	AV	N	E
DUNTK1059ECZA	1- 41	BT	N	E
//	2- 901	BT	N	E
DUNTK1059ECZZ	1- 41	BT	N	E
//	2- 901	BT	N	E
DUNTK1060ECZZ	1- 27	BN	N	E
//	3- 901	BN	N	E
【G】				
GCABA1009ECZZ	1- 43	AQ	N	D
GCABB1010ECZZ	1- 5	AT	N	D
GFTAA1267CCSA	1- 50	AB	N	D
GiTAZ1002ECZZ	1- 24	AF	N	C
GLEGP1009CCZZ	1- 45	AA		C
GLEGP1030CCZZ	5- 15	AB		C
GWAKP1041CCZZ	1- 49	AF		C
【H】				
HDECA1011ECZZ	1- 8	AF	N	D
HDECA1012ECZZ	1- 7	AE	N	D
【J】				
JKNBZ1952CCSA	1- 12	AM	N	C
JKNBZ1952CCSB	1- 13	AM	N	C
JKNBZ1952CCSC	1- 14	AM	N	C
【L】				
LANGK1005ECZZ	1- 33	AG	N	C
//	2- 1	AG	N	C
LANGK1006ECZZ	1- 31	AD	N	C
LANGK1007ECZZ	1- 47	AC	N	C
LBNDJ2003SCZZ	1- 20	AA		C
LHLDZ1002ECZZ	1- 1	AB	N	D
//	5- 1	AB	N	D
LHLDZ1003ECZZ	1- 2	AB	N	D
//	5- 2	AB	N	D
LPiN-1001ECZZ	1- 3	AB	N	C
LX-BZ1155CCZZ	1- 11	AA		C
LX-WZ1010ECZZ	1- 21	AA	N	C
【N】				
NSFTZ1001ECZZ	5- 3	AL	N	C
NSFTZ1002ECZZ	5- 3	AL	N	C
【P】				
PCAPH1013CCZZ	5- 13	AD		C
PSHEZ1144CCZZ	2- 3	AA		C
PSLDC1007ECZZ	1- 42	AF	N	C
PSLDC1008ECZZ	1- 29	AE	N	C
PTPEH1005ECZZ	1- 46	AF	N	C
PTPEH1006ECZZ	1- 9	AD	N	C
PTPEH1084CCZZ	1- 53	AA		C
【Q】				
QCNCM1295CC6J	1- 26	AV		C
//	3- 2	AV		C
QCNCM1338CC0B	1- 39	AA		B
//	2- 5	AA		B
QCNCM5016SC0G	1- 34	AB		C
//	2- 6	AB		C
QCNCW1004EC5J	2- 7	AS	N	C
QCNCW1006EC1G	1- 30	AN	N	C
QCNCW1007EC0G	1- 17	AE	N	C
//	4- 1	AE	N	C
QCNCW1008EC0B	1- 35	AB	N	B
QCNCW1293CCZZ	1- 25	AY		C
//	3- 1	AY		C
QCNTM1051CCZZ	2- 4	AB		C
QCNW-1011ECZZ	1- 40	AC	N	C
//	2- 8	AC	N	C
QJAKC1003CCZZ	1- 36	AD		B
//	2- 9	AD		B
QJAKC1013CCZZ	1- 38	AC		B
//	2- 10	AC		B
QJAKC1016CCZZ	1- 37	AC		C
//	2- 11	AC		C
QLUGE1005CCZZ	2- 12	AA		C
QPLGJ1022CCZZ	5- 4	AQ		C
QSW-M0131FCZZ	1- 16	AC		B
//	4- 2	AC		B

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK
QSW-S1074CCZZ	1- 15	AE		B
//	4- 3	AE		B
QTANZ1003ECZZ	1- 10	AC	N	C
【R】		BM		
RADPA1004ECZA	5- 5	BN	N	B
RADPA1004ECZB	5- 5	BN	N	B
RADPA1004ECZC	5- 5	BN	N	B
RADPA1004ECZD	5- 5	BN	N	B
RADPA1004ECZE	5- 5	BN	N	B
RADPA1004ECZF	5- 5	BN	N	B
RADPA1004ECZG	5- 5	BN	N	B
RADPA1004ECZH	5- 5	BN	N	B
RADPA1004ECZi	5- 5	BN	N	B
RADPA1004ECZJ	5- 5	BN	N	B
RADPA1004ECZK	5- 5	BM	N	B
RADPA1004ECZL	5- 5	BN	N	B
RADPA1004ECZZ	5- 5	BM	N	B
RC-CZ1021CCZZ	2- 13	AB		C
RC-CZ1039CCZZ	2- 14	AB		C
RC-CZ1077CCZZ	2- 15	AC		C
RCiLZ1032CCZZ	2- 2	AD		C
RFiLN1008CCZZ	2- 16	AH		C
RRLYZ2400QCZZ	2- 17	AP		B
【S】				
SPAKA0050ECZZ	5- 8	AK	N	D
SPAKA0178ECZZ	5- 10	AD	N	D
SPAKA0179ECZZ	5- 11	AC	N	D
SPAKA146ACCZZ	5- 12	AB		D
SPAKC0094ECZZ	5- 9	AK	N	D
【T】				
TCAUK1191CCZZ	5- 14	AA		D
TiNSE1032ECZZ	5- 6	AR	N	D
TiNSM1033ECZZ	5- 6	BC	N	D
【U】				
UBAGZ1001ECZZ	5- 7	AZ	N	D
UBATN1003ECZZ	1- 32	BA	N	A
【V】				
VCEAGU1AW107M	2- 18	AB		C
VHDDAN202K/-1	2- 19	AC		C
VHDDS1588L2-1	2- 20	AB		B
VHDRK13////-1	2- 21	AF	N	B
VHDRM10Z///-1	2- 22	AC	N	B
VHD11DQ03//-1	2- 23	AE		B
VHEHZ5C1///-1	2- 24	AB		B
VHiLB1247//-1	2- 25	AM		B
VHiLR38045/-1	2- 26	AQ	N	B
VHi53257F5216	2- 27	AU	N	B
VRS-TP2BD473J	2- 28	AA		C
VRD-RB2HY100J	2- 29	AA	N	C
VRS-TP2BD102J	2- 30	AA		C
VRS-TP2BD103J	2- 31	AA		C
VRS-TP2BD104J	2- 32	AA		C
VRS-TP2BD105J	2- 33	AA		C
VRS-TP2BD123J	2- 34	AA		C
VRS-TP2BD330J	2- 35	AA		C
VRS-TP2BD681J	2- 36	AA		C
VRS-TP2BD682J	2- 37	AA		C
【X】				
XBBSD20P06000	1- 28	AA		C
//	2- 38	AA		C
XBBSD20P08000	2- 39	AA		C
//	3- 3	AA		C
XBBSD20P10000	3- 4	AA		C
XBBSM20P06000	1- 52	AA		C
XBSSM20P06000	1- 4	AA		C
XNESD20-16000	2- 40	AA		C
//	3- 5	AA		C
XUBSD20P04000	1- 23	AA		C
XUBSD20P06000	1- 19	AA		C
XUBSD26P06000	1- 48	AA		C
XUBSD26P08000	1- 44	AA		C
【0】				
00PDG206/////	6- 42	AU		C
00PDG214/////	6- 5	AN		C
00PDG216/////	6- 19	AR		C
00PDG217/////	6- 21	AR		C
00PDG218/////	6- 9	AR		C
00PDG219/////	6- 10	AN		C
00PDG223/////	6- 39	AQ		C
00PDG224/////	6- 31	BG		C

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
00PDG236/////	6- 103	AK		C	
00PDG237/////	6- 38	AK		C	
00PDG240/////	6- 41	AN		C	
00PDG249/////	6- 3	BB		C	
00PDG250/////	6- 16	BK		B	
00PDG259/////	6- 101	AY		C	
00PDG260/////	6- 32	AZ		C	
00PDG262/////	6- 40	AW		C	
00PDG265/////	6- 17	BB		C	
00PDG275/////	6- 1	BA		C	
00PDG276/////	6- 50	AP		B	
00P01G0549///	6- 44	AG		C	
00P01G0557///	6- 2	AR		C	
00P01G0703///	6- 43	AN		C	
00P07G0247///	6- 4	AL		C	
00P07G247////	6- 18	AL		C	
00P10G0493///	6- 11	AR		C	
00P11G0178///	6- 61	AD		C	
00P11G0179///	6- 60	AD		C	
00P12G0204−11	6- 24	AE		C	
00P13G0547−04	6- 48	AN		C	
00P13G0549///	6- 49	AF		C	
00P13G0554///	6- 47	AC		C	
00P13G0559///	6- 102	AD		C	
00P17G0028///	6- 7	AR		C	
00P17G0029///	6- 6	AR		C	
00P19G0365///	6- 23	AC		C	
00P19G0367///	6- 8	AD		C	
00P19G0369///	6- 20	AD		C	
〃	6- 22	AD		C	

PARTS CODE	NO.	PRICE RANK	NEW MARK	PART RANK	
00P19G0370///	6- 36	AD		C	
00P19G0372///	6- 46	AD		C	
00P19G0381///	6- 52	AC		C	
00P19G0391///	6- 25	AD		C	
00P23−0057///	6- 57	AA		C	
00P23G0049///	6- 58	AE		C	
00P23G0056−01	6- 30	AC		C	
00P24−0008−00	6- 63	AC		C	
00P27−0002−19	6- 14	AA		C	
00P27−0003−19	6- 29	AA		C	
00P27−0006−19	6- 15	AB		C	
00P30−0307−00	6- 13	AA		C	
00P30−0309−00	6- 12	AC		C	
00P30−0312−00	6- 53	AC		C	
00P30−0409−00	6- 27	AA		C	
00P30−4C08−00	6- 64	AB		C	
00P34L0309−00	6- 45	AC		C	
00P62−0010///	6- 51	AG		B	
00P63G4021///	6- 59	AP		C	
00P68G1179///	6- 62	AK		C	
00P72−0012///	6- 104	AT		C	
00P72−0013///	6- 105	AT		C	

Parts code		Voltage(V)	Type of plug	Country
RADPA1004ECZZ	U.S.A.	120	Flat 2-p	U.S.A.
" ZY	Canada	120	Flat 2-p	Canada
" ZA	MV	220	Round (SEV) 2-p	Germany, Finland, Sweden, Norway, Denmark, Switzerland (SEV)
" ZB	MB	240	——	England
" ZC	MA	240	Square (NSW) 2-P	Australia, New Zealand, Fiji
" ZD	SH	220	Round 2-p	Republic of South Aflica
" ZE	SE	200	Round 3-p	Hong Kong
" ZF	SB	220	Round 2-p	Rumania, Spain, Turkey, U.S.S.R, Yugoslavia, Argentina, Bolivia, Brazil, Austria, Belgium, Bulgaria, Czechoslovakia, France, Chile, Paraguay, Peru, Uruguay, French Guiana, Guadeloupe, Greece, Netherlands, Hungary, Iceland, Italy, Poland, Portugal, Afghanistan, Thailand, Burme, India, Indonesia, Iran, Iraq, Jordan, Lebanon, Nepal, Pakistan, Qatar, Algeria, Dahomey, Ethiopia, Ghana, Republic of the Ivory Coast, Cameroun, Kenya, Malawi, Mali, Rwanda, Sudan, Togo, Tunisia, Yemen, Bangladesh, Mozambique, Libya, Congo, Angola, The United Arab Emirates, S.R. of Viet Nam.
" ZG	SC	110	Flat 2-p	Taiwan, Jamica, Liberia, Guam
" ZH	SK	240	Round 2-p	Kuwait, Zambia, Uganda
" ZI	SN	127/220	Flat 2-p	Saudi Arabia
" ZJ	SM	240	Square 3-p	Singapore, Malaysia
" ZK	SJ	220	Flat 2-p	Honduras, Philippines
" ZL	SD	120	Flat 2-p	Republic of Panama, El Salvador, Trinidad and Tobago, Colombia, Nicaragua, Venezela, Mexico, Bermuda, Costa-Rica, Dominica, Ecuador, Guyana, Guatemala, Barbados.

MODEL CE-1600F

- 2.5" floppy disk drive
- Since individual parts replacement is not possible with this model, when a failure is discovered after the test mention in Section 7, Test program, the unit must be replaced with new one.

1. Specifications

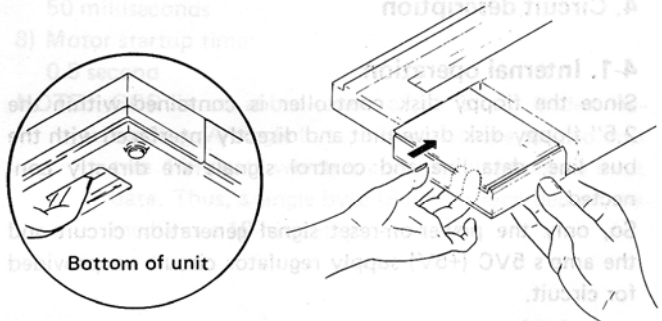
Model name: CE-1600F
Product name: Floppy disk drive
Drives: One drive (one side)/unit
Recording media: 2.5" two-sided floppy disk
Recording method: GCR (4/5)
Tracks: 16 tracks/side
Capacity: 64KB (one side)
(8 sectors/track)
Power supply: 6VDC: Supplied from the unit connected.
Power consumption: 2.5W
Operating temperature: 10°C ~ 35°C
(drive operating requirement)
Humidity: 20% ~ 80% (without moisture condensation)
Physical dimensions: 96mm(W) x 122mm(D) x 39mm(H)
Weight: 470 grams
Accessories: 2.5" two-sided floppy disk (x 1), instruction book (x 1)
Option: CE-1650F
(contents of 10 2.5" two-sided floppy disks)

NOTE: '2.5" (63.5 mm)' indicates the diameter of the floppy disk media.

2. Cautions in installing and removing the CE-1600F

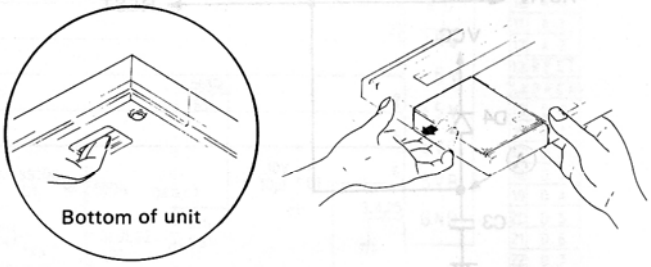
2-1. Cautions in installing the CE-1600F

Power must be shut off to the CE-1600P before connecting the CE-1600F to the CE-1600P.
Pay special attention to hold the unit in a way as shown in the figure below with care not to touch the disk holder, in order to avoid a read/write failure because of center deviation.

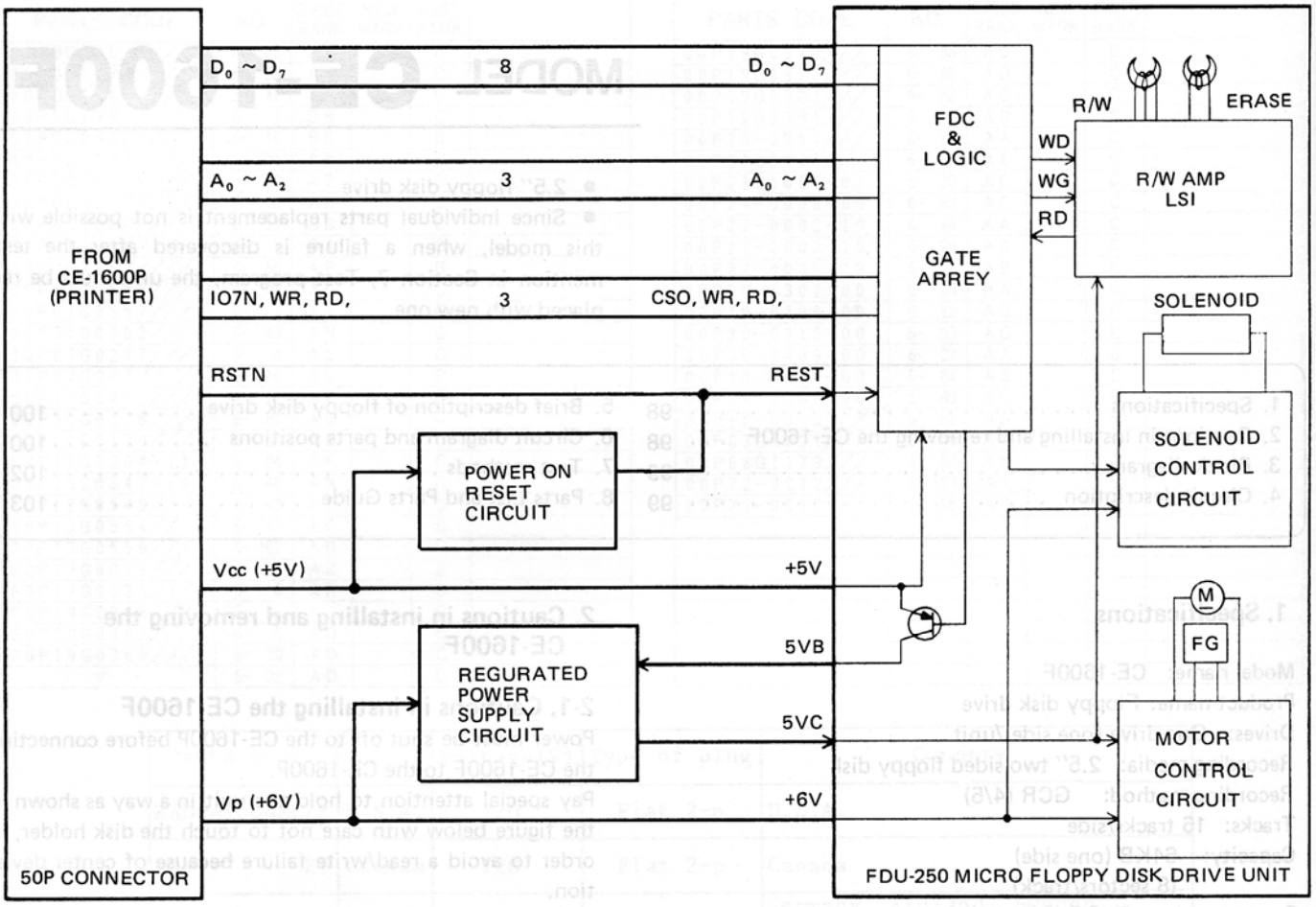


2-2. Cautions in removing the CE-1600F

Before the removal of the CE-1600F, make sure that the power is off and remove it without adding force to the disk holder (see the figure below).



3. Block diagram



4. Circuit description

4-1. Internal operation

Since the floppy disk controller is contained within the 2.5" floppy disk drive unit and directly interfaced with the bus line, data line and control signals are directly connected.

So, only the power-on-reset signal generation circuit and the amp's 5VC (+5V) supply regulator circuit are provided for circuit.

4-2. Power-on-reset signal generation circuit

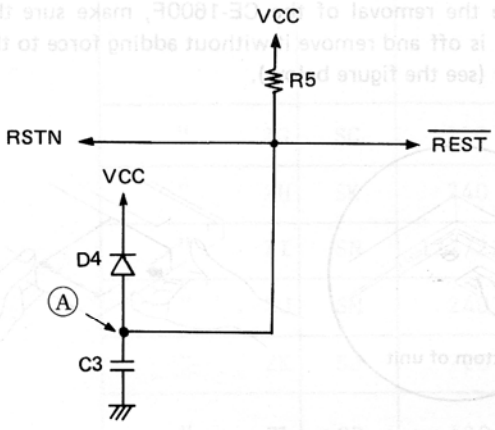


Fig. 1 Reset circuit

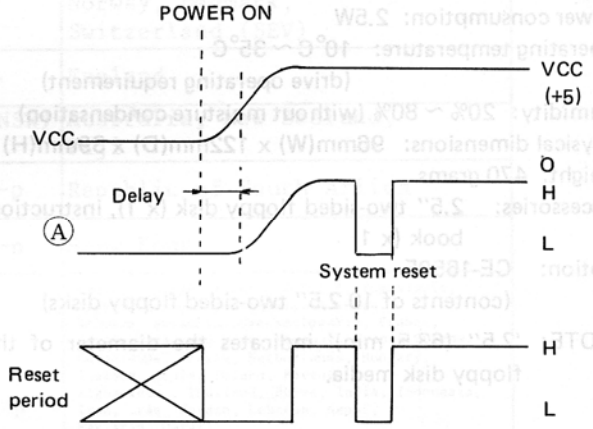


Fig. 2 Reset timings

Fig. 1 shows the reset circuit and Fig. 2 shows its timings. R5 is a charge current regulating resistor C3 which is used for pullup and delay. D4 is a diode which is used to bypass the charge in C3 to VCC line when VCC is off.

The reason why the reset signal is required at power on is to hold it in the standby mode so as to avoid malfunction in the floppy disk controller inside the floppy disk unit.

4-3. Regulated power supply circuit

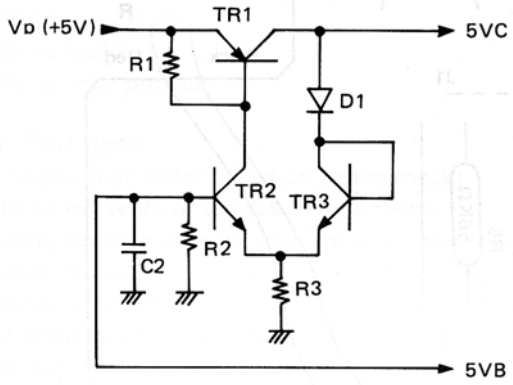


Fig. 3 Regulated power supply circuit

Fig.3 shows the regulated voltage supply circuit. In this circuit, floppy disk unit's 5VC (5V of amp) is supplied from VP (battery voltage), because 5VC can not be supplied from VCC on account of current restriction.

For the voltage of 5VC is used with a voltage difference of 0.5V minimum against VCC, the power is produced in reference to 5VB through the differentiation circuit composed of TR2 and TR3, not merely the regulator circuit. 5VB is a transistor output which is employed to turn on/off VCC with the MOTOR ON signal, and it has less voltage drop caused in the transistor, as compared with VCC. So, D1 is inserted to the output voltage feedback transistor TR3 to correct 5VC to be 0.2 to 0.3 volts higher then 5VB in appearance. (A schottky barrier diode is used for D1.)

5. Brief description of floppy disk drive

The floppy disk controller is implemented within the 2.5" floppy disk drive, and the floppy disk driving and head seeking are done by one motor. The floppy disk is driven by the belt and the head is seeked using the solenoid and cam.

The floppy disk controller and its peripheral logic are contained in a single chip gate array (2700 gates) and the read/write amplifier is also in a single chip LSI, which are directly bus connected to permit a low voltage driving.

Floppy disk format and write method are unique to the floppy disk. Though the floppy disk drive is for one-sided operation, both sides of the media can be used.

Specification of FDU 250

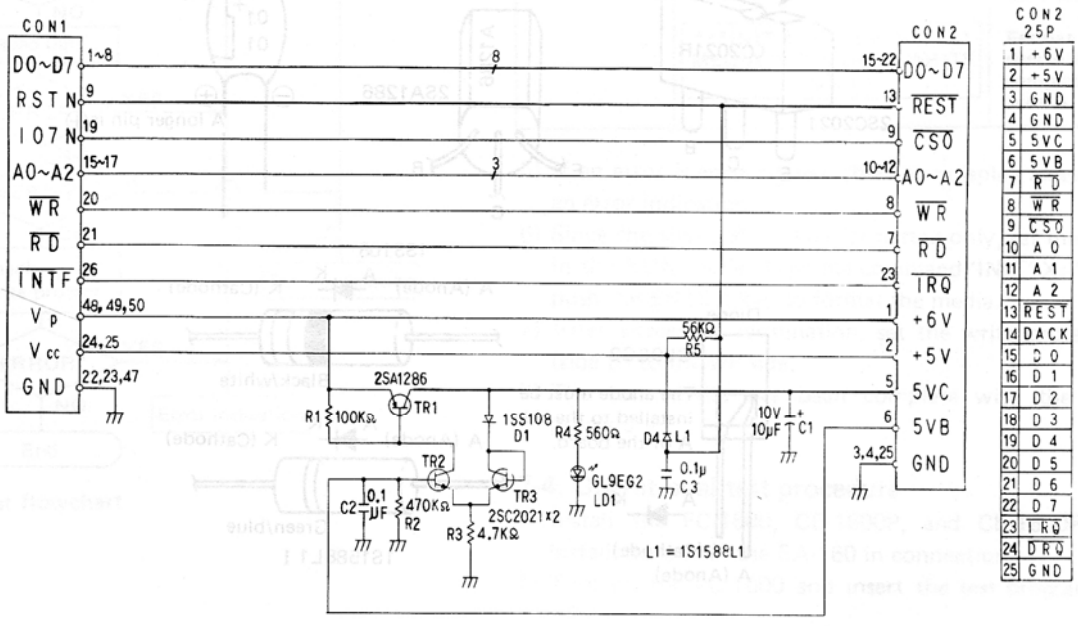
1) Memory capacity:
   64KB (512 Bytes/sector, 8 sectors/track)
2) Recording method:
   GCR (4/5)
3) Transfer speed:
   250K bits (25K Bytes/sec)
4) Track density:
   48 TPI
5) Total tracks:
   16
6) Revolutions:
   270 rpm
7) Access time:
   One step 80 milliseconds from track 00 to track 15.
   170 milliseconds to restore from track 15 to track 00.
   Settling time:
   50 milliseconds
8) Motor startup time:
   0.5 second

NOTE: GCR is an abbreviation of of Group Coded Recording. A single byte, 8 bits, data are divided into two 4-bit data which is also converted onto a 5-bit data. Thus, a single byte (8 bits) is recorded on the media as a 10-bit data.

6. Circuit diagram and parts positions

CON1 50P

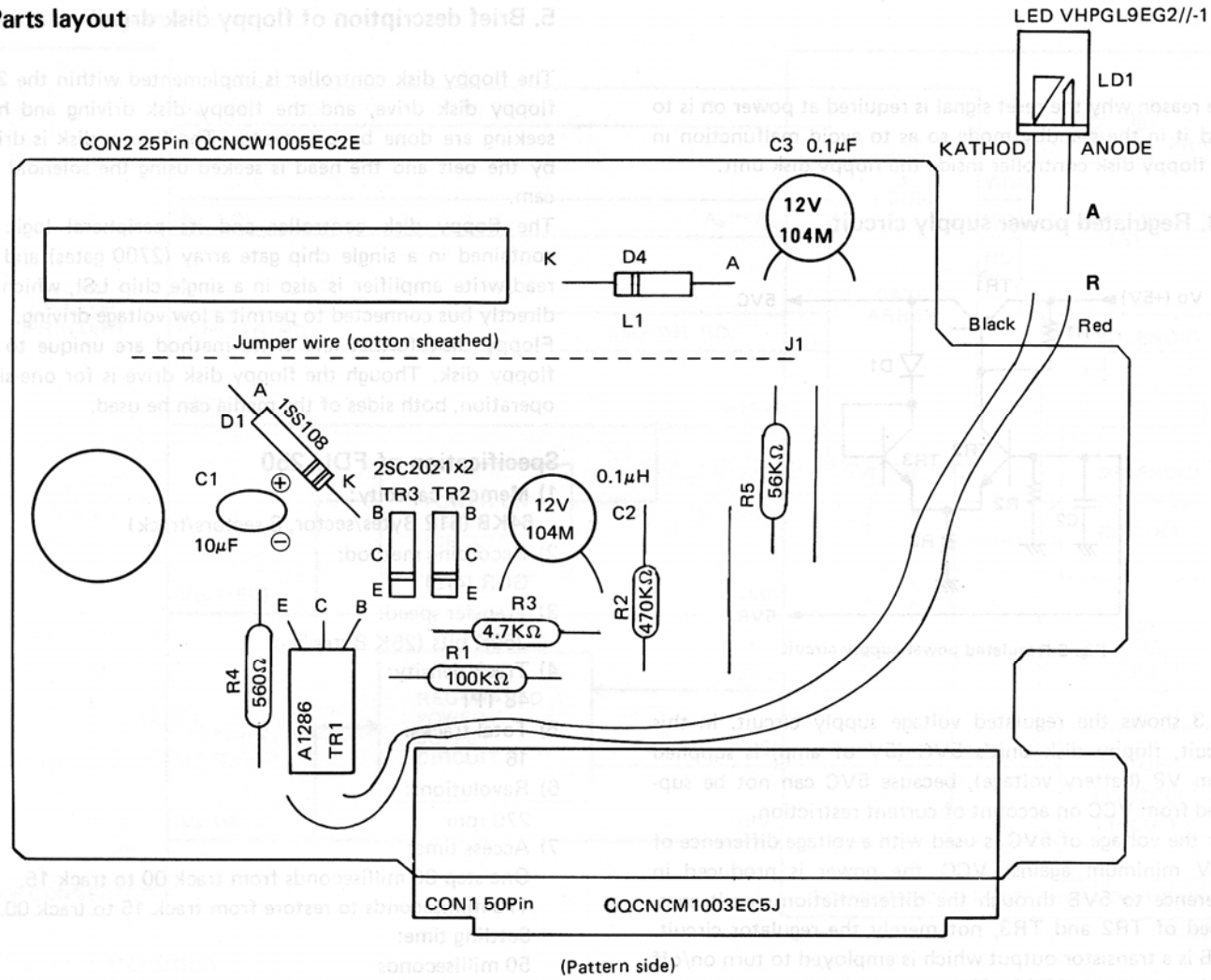
26	INTF	D 7	1
27	Vcc	D 6	2
28	M 1	D 5	3
29	CLK	D 4	4
30	P T	D 3	5
31	P U	D 2	6
32	P V	D 1	7
33	FGND	D 0	8
34	FGND	RSTN	9
35	A 8	A 7	10
36	A 9	A 6	11
37	A10	A 5	12
38	A11	A 4	13
39	A12	A 3	14
40	A13	A 2	15
41	A14	A 1	16
42	A15	A 0	17
43	BFO	MREQ	18
44	IORQ	IO7N	19
45	WAIT	WR	20
46	ELH	RD	21
47	GND	GND	22
48	Vp	GND	23
49	Vp	Vcc	24
50	Vp	Vcc	25



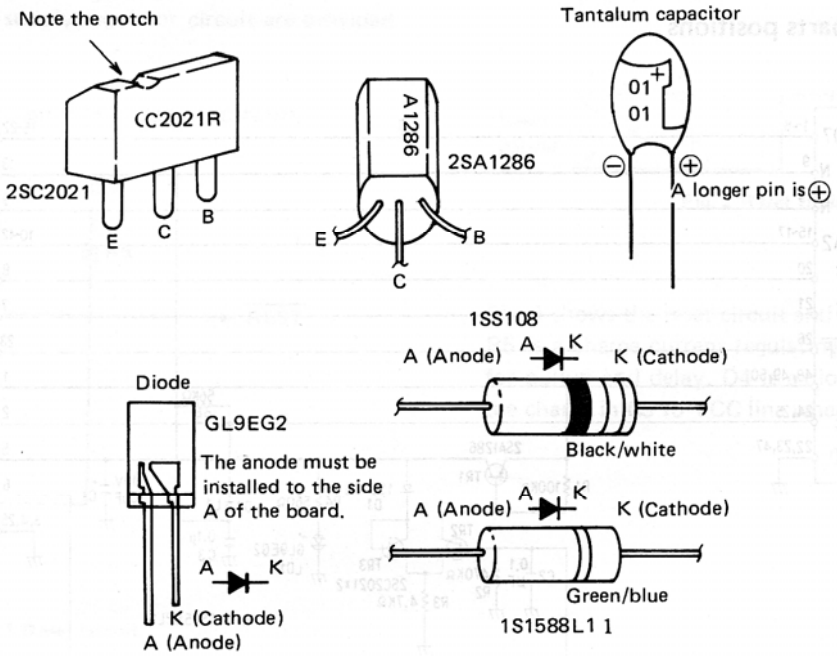
CON2 25P

1	+6V
2	+5V
3	GND
4	GND
5	5VC
6	5VB
7	RD
8	WR
9	CS0
10	A0
11	A1
12	A2
13	REST
14	DACK
15	D0
16	D1
17	D2
18	D3
19	D4
20	D5
21	D6
22	D7
23	IRQ
24	DRQ
25	GND

Parts layout



NOTE: Slack in the jumper (J1) must be treated in the opposite direction as the 25-pin connector, because the rib is provided between the connector and J1.



7. Test methods

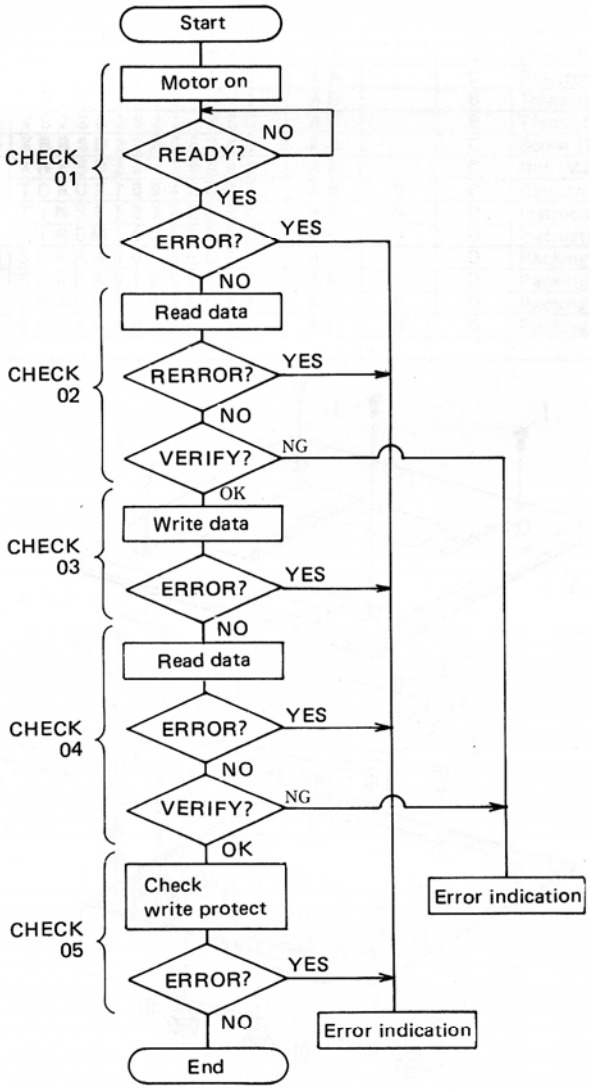
As the 2.5" floppy disk drive used in the CE-1600F incorporates the floppy disk controller within the drive unit, it operates as an external memory unit of the I/O space as seen from the PC-1600.
The following five test items are tested.

1) Motor on/off
2) Head seek
3) Sector read/write
4) Sense media
5) Sense write protect

7-1. Test items

1) Detection of motor on action (ready check)
2) Read and verify of the data on the media
3) Write test data onto the media without write protect
4) Read and verify of the data on the media, again
5) Sense write protect

Test results are represented by the status register and IOCS error code.



Test flowchart

7-2. Items required

1) PC-1600
2) CE-1600P
3) CE-1600F
4) EA-160
5) Test program stored media (UKOGC3018CSZZ)
6) Test media which has been prepared by the data write program.
7) Printout paper

7-3. Preparing test media

The test media required for the test can be prepared in the following way:

1) Install the PC-1600, CE-1600P, and CE-1600F (test installation) with the EA-160 in connection.
2) Turn on the PC-1600 and insert the test program contained media.
3) Type the command 'LOAD"X:WMEDIA"' and push the ENTER key.
4) When the prompt symbol appears, remove the test program stored disk and ensure that the machine is in the RUN mode. Next, type the command 'R.(RUN)', then push the ENTER key.

Step	Display message	Note
RUN ENTER	***INIT & DATA WRITE*** SET BLANK MEDIA & HIT [ENTER] KEY!!	Set the blank media (CE-1650F).
Set the side A of a blank disk (CE-1650F).		
ENTER	Set diskette for X: MEDIA INTIALIZE NOW!!	The green access lamp of the CE-1600F comes active for 5 seconds.
ENTER	***INIT & DATA WRITE*** MEDIA INITIALIZE NOW	The green LED comes active for 20 seconds.
	INIT & DATA WRITE WRITE DATA NOW!!	The green LED comes active for 3 seconds.
	INIT & DATA WRITE DATA READ NOW!!	The green LED comes active for 7 seconds.
	INIT & DATA WRITE MEDIA INIT & DATA WRITE OK!!	Format and data write are completed (side A).

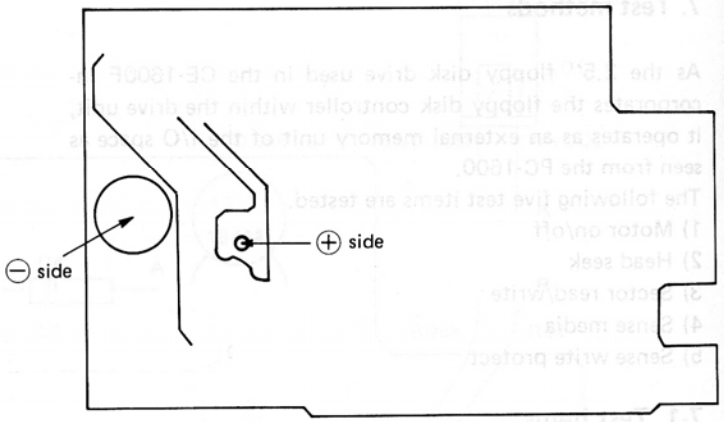
5) If an error is encountered, check the display message for an error indication.
6) Since the side B should be formatted only, set the media in the RUN mode. Type the command 'INIT"X:"', then push the ENTER key to format the media.
7) After successful termination, set the write protect tab (side B) to the WP side.
8) The test media has been complete with the above procedure.

7-4. Operational test procedure

1) Install the PC-1600, CE-1600P, and CE-1600F (test installation) with the EA-160 in connection.
2) Turn on the PC-1600 and insert the test program con-

tained media.

3) Type the command 'LOAD"X:CE-1600F"' and push the ENTER key.
4) When the prompt symbol appears, remove the test program stored disk and turn off the PC-1600.
5) Disconnect the test installation CE-1600F from the CE-1600P.
6) Connect the CE-1600F to be tested with the CE-1600P.
7) Turn on the PC-1600.
8) Type the command 'R.(RUN)', then push the ENTER key.
9) When the prompt is issued for setting of the media, insert the test media with the side A face up.
10) Push the ENTER key. If other key is pushed, the test resumes from 8).
11) After continuous test of test items, 1 thru 4, "OK" is displayed when the test has been successful. If not successful, the error is indicated on the display and the printer.
12) After successful ending of test items, 1 thru 4, remove the test media and set the side B of the media whose write protect tab is set to WP.
13) Push the ENTER key now to check the function of the write protect switch. If it has been successful, the description is printed and the test terminates.
14) During this write protect test period, measure the +5VC check point of the interface board with the dc voltmeter to check that it is within a range of 4.5VDC to 5.5VDC (5V±0.5V).



5VC voltage test location (pattern side)

7-5. Write protect test

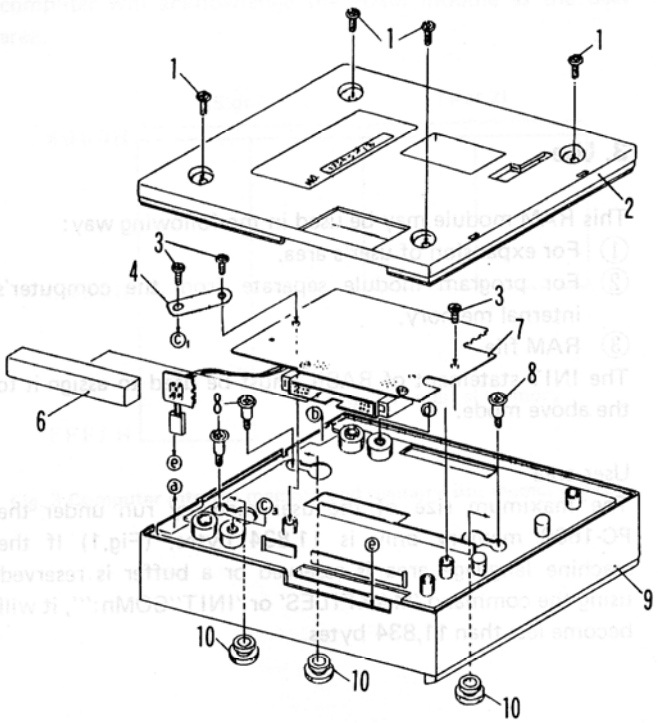
This test is conducted to check proper functioning of the write protect of the floppy disk drive.

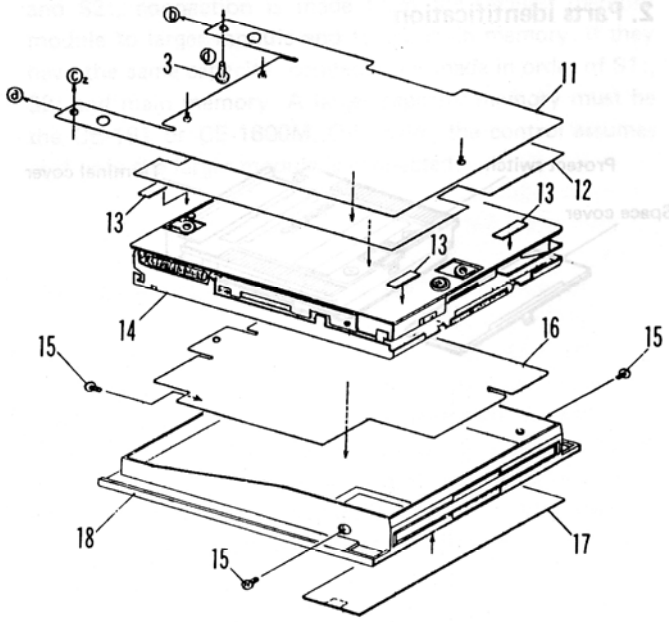
- Test description
  - Check class 05 (CHECK 05)
    Insertion of the media is checked after the motor has turned on and functioning of the write protect is checked. That is, it checks that it is the media that write protected.
- Check items
  1) During the test (while the access LED is active), measure the voltage across pads at two locations of the pattern side using the dc voltmeter (6 to 10VDC) to ensure that it is 5VDC±0.5VDC (4.5V ~ 5.5V).
  2) When the access lamp goes out, make sure that 5VC is now turned to 0V.
  3) After completion of the test, check the display message on the PC-1600 that "OK" is on display.

8 PARTS LIST & GUIDE

1 Exteriors

NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	XUBSM26P08000	AA	N	C	Screw (2.6×8)
2	DUNTG1051ECZZ	AP	N	D	Bottom cabinet unit
3	XUBSD26P06000	AA		C	Screw (2.6×6)
4	QEARP1002ECZZ	AA	N	C	Earth plate
6	PCAPH1002ECZZ	AB	N	C	Connector cap
7	DUNTK1052ECZZ	BC	N	E	Interface PWB unit (This includes №101~116)
8	LX−BZ1009ECZZ	AB	N	C	Screw
9	GCABB1006ECZZ	AK	N	D	Top cabinet
10	PGUMM1006ECZZ	AB	N	C	Rubber
11	PSLDC1005ECZZ	AE	N	C	Shield plate A
12	PSHEP1008ECZZ	AB	N	C	Insulator sheet B
13	PTPEZ1003ECZZ	AB	N	C	Shield plate fixing tape
14	DUNT−1041ECZZ	BZ	N	E	2.5inch FD unit
15	LX−BZ1008ECZZ	AA	N	C	Screw
16	PSLDC1006ECZZ	AD	N	C	Shield plate B
17	HDECA1008ECZZ	AC	N	D	Dec. panel
18	GCOVH1001ECZZ	AH	N	D	Cover
101	QCNCM1003EC5J	AP	N	C	Connector (50pin)
102	QCNCW1005EC2E	AF	N	C	Connector (25pin)
103	VCTYPU1NX104M	AB		C	Capacitor (12WV 0.10μF)
104	VCSATU1AE106M	AD		C	Capacitor (10WV 10μF)
105	VHDDS1588L2−1	AB		B	Diode (DS1588L2)
106	VHD1SS108//−1	AB		B	Diode (1SS108)
107	VHPGL9EG2//−1	AB	N	B	Photo transistor (GL9EG2)
108	VRD−ST2EY104J	AA		C	Resistor (1/4W 100KΩ ±5%)
109	VRD−ST2EY472J	AA		C	Resistor (1/4W 4.7KΩ ±5%)
110	VRD−ST2EY474J	AA		C	Resistor (1/4W 470KΩ ±5%)
111	VRD−ST2EY561J	AA		C	Resistor (1/4W 560Ω ±5%)
112	VRD−ST2EY563J	AA		C	Resistor (1/4W 56KΩ ±5%)
113	VS2SA1286−/−1	AD		B	Transistor (2SA1286)
114	VS2SC2021−RSC	AF		B	Transistor (2SC2021−RSC)
115	XBBSD20P08000	AA		C	Screw (2×8)
116	XNESD20−16000	AA		C	Nut (M2)
201	TCAUZ1004ECZZ	AB	N	C	Caution card
202	TiNSE1034ECZZ	AS	N	D	Instruction book (USA only)
	TiNSM1035ECZZ	BA	N	D	Instruction book (E,F,G,S,I)
203	SPAKA0056ECZZ	AK		D	Packing cushion
204	SPAKA0100ECZZ	AL	N	D	Packing cushion for set
205	SPAKA0124ECZZ	AC	N	D	Packing cushion for media
206	SPAKC0092ECZZ	AG	N	D	Packing case





MODEL CE-1600M

- 32KB RAM module

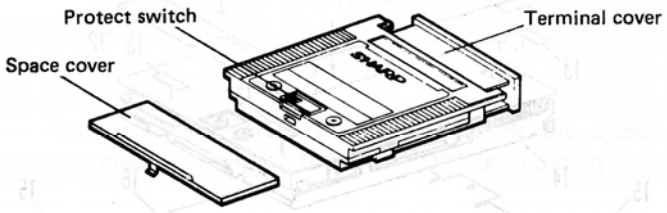
1. Specifications

Product name: Program module
Model name: CE-1600M
Type: Module (RAM)
Capacity: 32KB
Backup battery: 3V(DC) lithium battery (CR2032 x 1)
Battery life: About 5 years in the pocket computer, or, about 24 month when removed from the pocket computer under temperature of 20°C. (Subject to variation depending on the usage and environment.)
Operating temperature: 0 to 40°C
Physical dimensions: 40.9mm (W) x 42.8 mm (D) x 8.5 mm (H)
Weight: 15 grams, including the battery cell
Accessories: Case, cover label (x 3), space cover, lithium battery (in the main unit), instruction book.

Protect switch
When the switch is set to the side marked with "●", memory write is prohibited so that it disables to write, erase, and revise the memory contents.
When the switch is at the side not marked, the write protect is cleared.

* When it has been write protected, cover the switch with the cover label to avoid incidental manipulation of the switch.

2. Parts identification



3. Use

This RAM module may be used in the following way:

① For expansion of user's area.
② For program module separate from the computer's internal memory.
③ RAM file

The INIT statement of BASIC must be used to assign it to the above mode.

User area
The maximum size of the user memory run under the PC-1600 memory only is 11,834 bytes. (Fig.1) If the machine language area is reserved or a buffer is reserved using the command 'MAXFILES' or 'INIT"COMn:"', it will become less than 11,834 bytes.

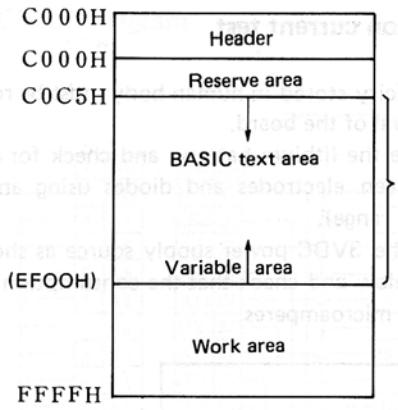


Fig. 1 Bank 0 user area map

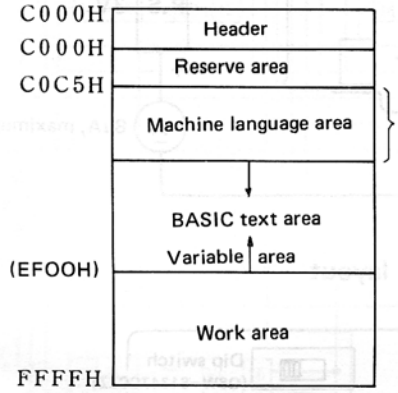


Fig. 2 Bank 0 user area map

Expansion of user area

When "M" is specified with the INIT statement after connecting the RAM module into the memory slot, the computer will acknowledge the RAM module as the user area.

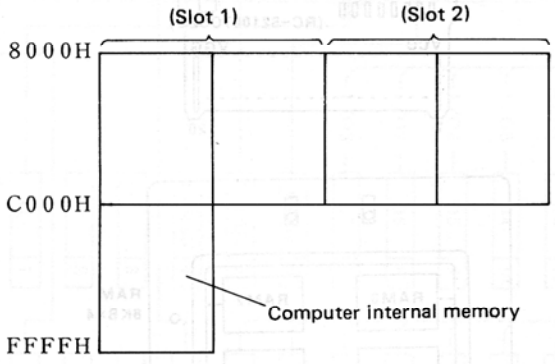
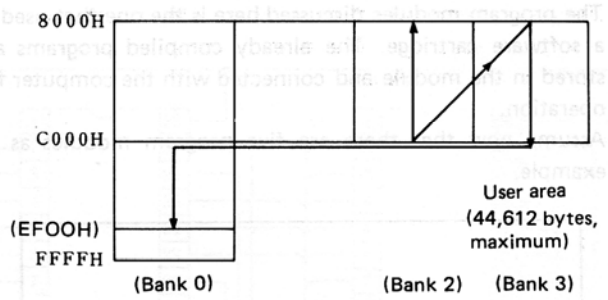
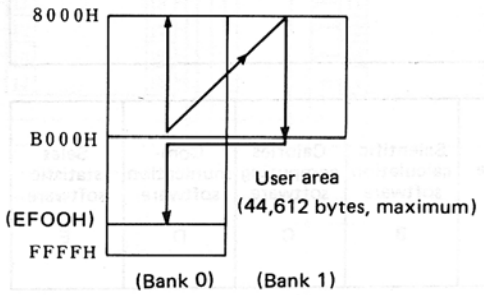


Fig. 3 Computer internal memory and memory slot memory map

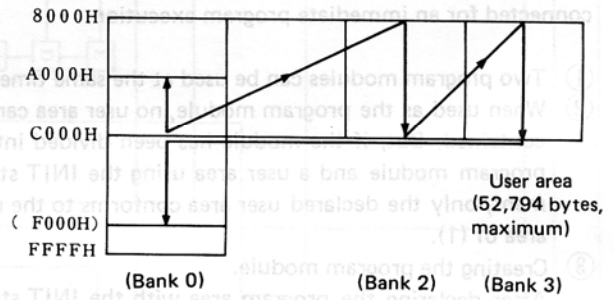
When the CE-1600M is connected to S2:



When the CE-1600M is connected to S1:



When the CE-159 is connected to S1: and the CE-1600M is connected to S2:

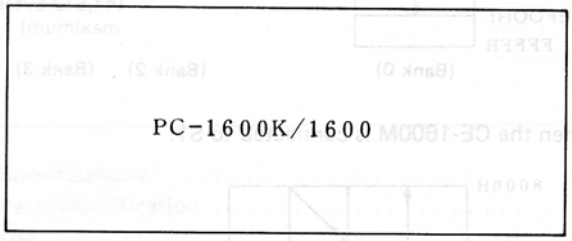


When the RAM module is connected to both slots of S1: and S2:, connection is made from the smallest memory module to larger module and to the main memory. If they have the same capacity, connection is made in order of S1:, S2: and main memory. A larger capacity memory must be the CE-161 or CE-1600M. Otherwise, the control assumes as if only the larger module is connected.

Program module

The program modules discussed here is the one that used as a software cartridge. The already compiled programs are stored in the module and connected with the computer for operation.

Assume now that there are five program modules as an example.



Game software	Scientific calculation software	Calories computing software	Com-munication software	Seles statistic software
A	B	C	D	E

Program modules

According to the need, the desired program module is connected for an immediate program execution.

① Two program modules can be used at the same time.
② When used as the program module, no user area can be contained. But, if the module has been divided into a program module and a user area using the INIT statement, only the declared user area conforms to the user area of (1).
③ Creating the program module.
After declaring the program area with the INIT statement, the program is written or loaded to that area.
④ The memory protected CE-159, CE-161, or CE-1600M must be used for the program module.

RAM file module

With this usage, the completed program or data are saved into the memory module, to be loaded onto the user area when so required.

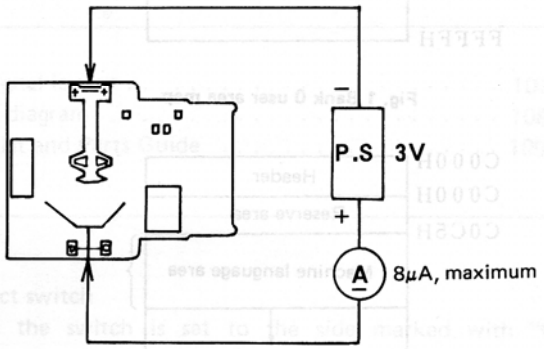
If used as a RAM module, the module is not included in the area.

① The module that can be used the RAM file module is the CE-161 and CE-1600M.
② The RAM file module can be accessed free from the main unit. While it is removed from the main unit, the contents are retained by the internal battery.

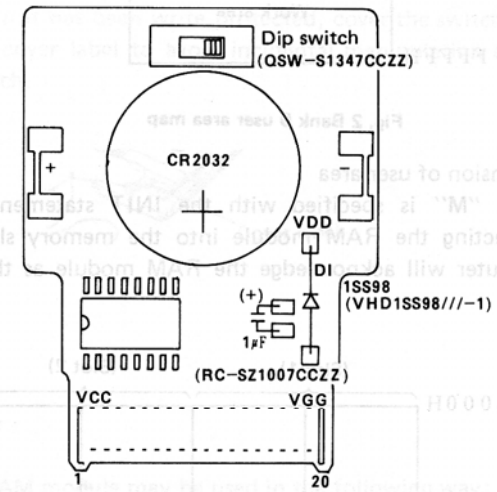
- What program and data are contained within the RAM file module can be known by means of the FILES statement or LFILES statement. It is possible to change the name or delete the program or data.

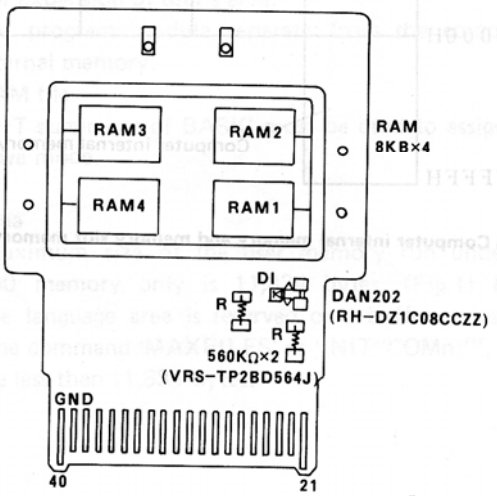
4. Consumption current test

1. Static electricity stored in human body must be released before removal of the board.
2. First, remove the lithium battery, and check for a short circuit between electrodes and diodes using an ohmmeter (R x 1 range).
3 Connected the 3VDC power supply source as shown in the figure below and check that the consumption power is less than 8 microamperes.

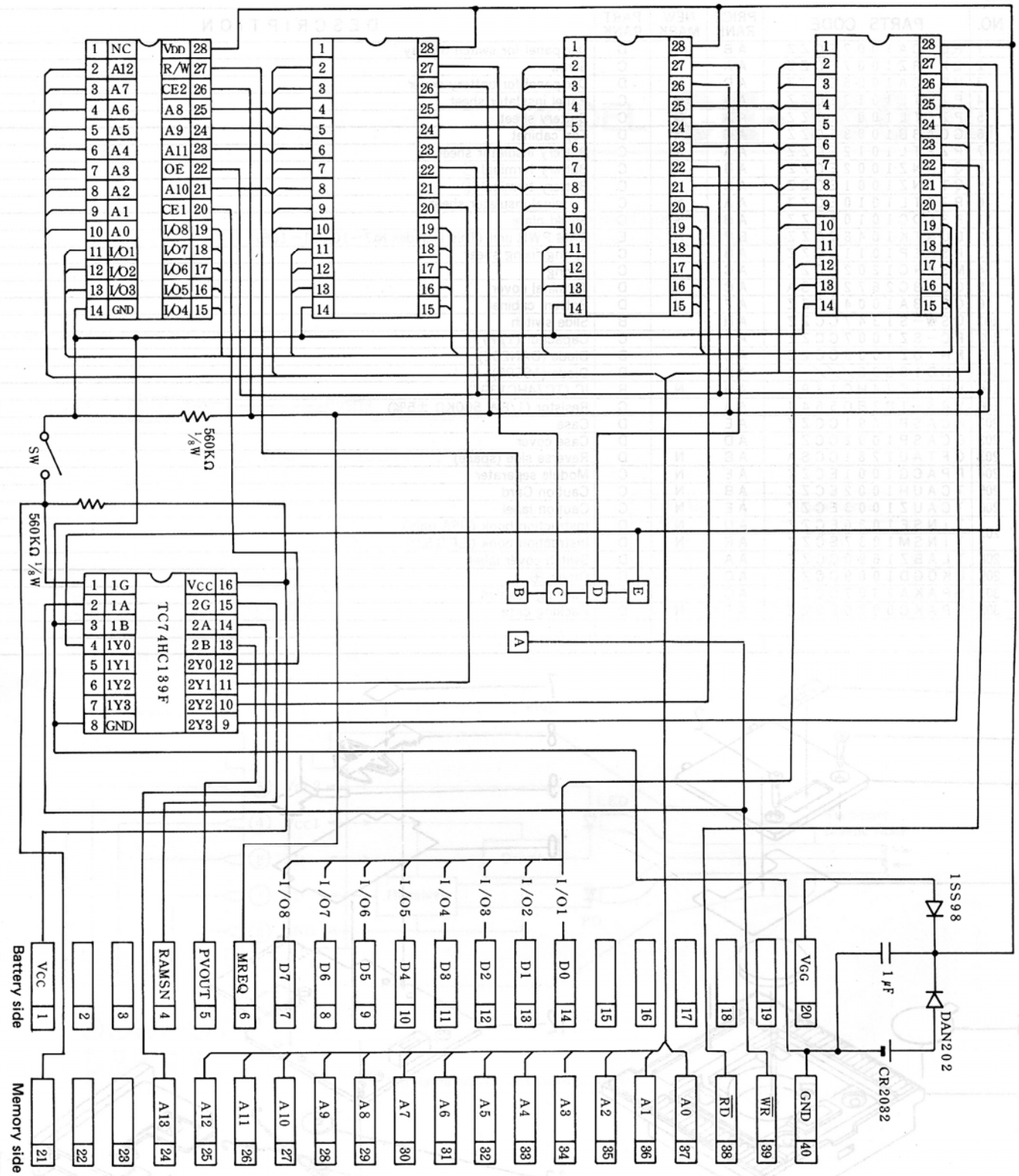


5. Parts signal layout





6. Circuit diagram

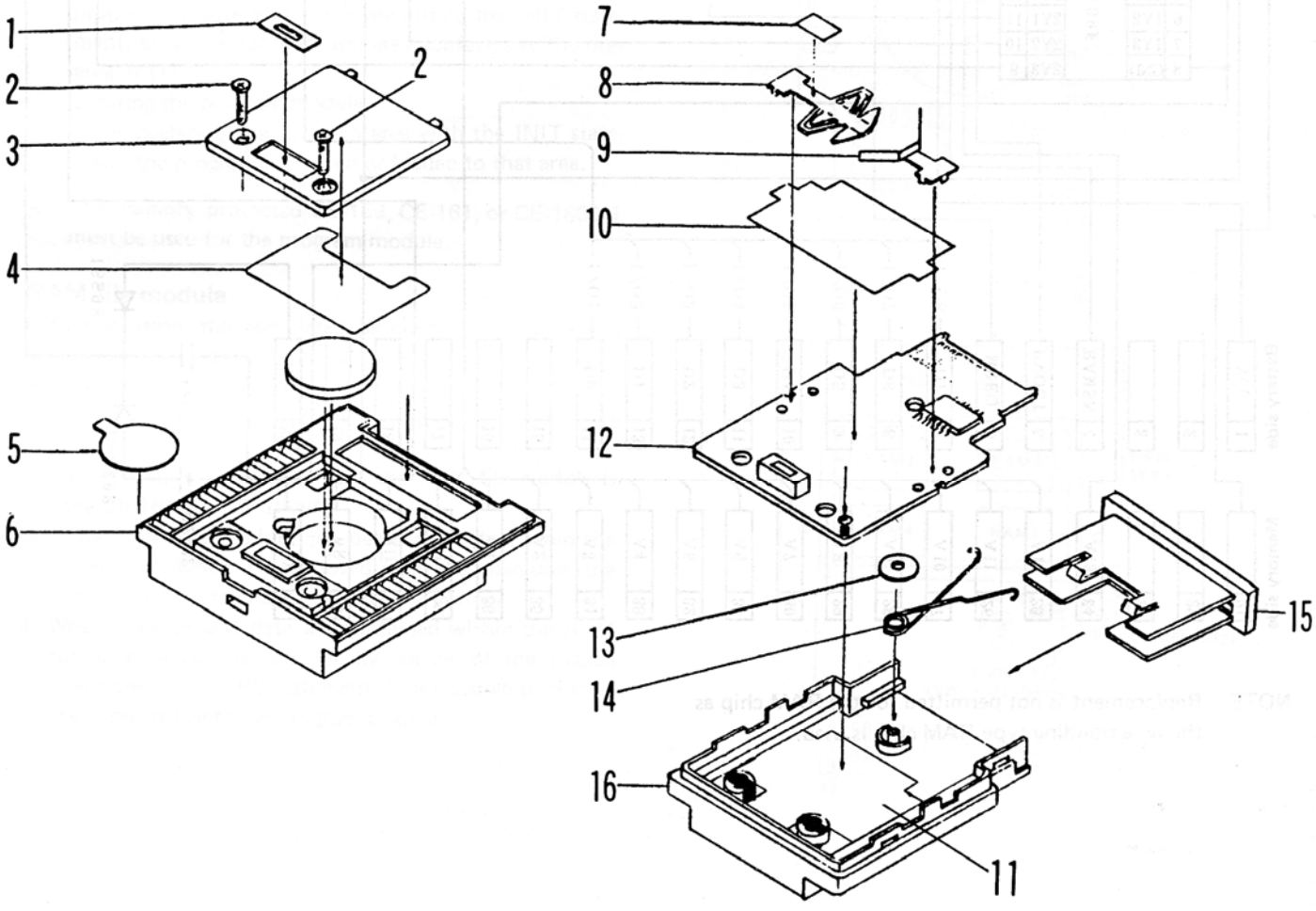


NOTE: Replacement is not permitted for the RAM chip as the wire bonding type RAM chip is used.

7. PARTS LIST & GUIDE

Exteriors

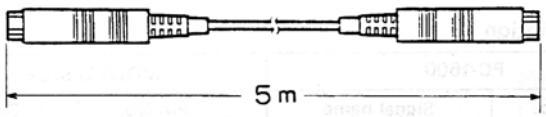
NO.	PARTS CODE	PRICE RANK	NEW MARK	PART RANK	DESCRIPTION
1	HDECA1007ECZZ	AB	N	D	Dec.panel for switch display
2	LX-BZ1007ECZZ	AA	N	C	Screw
3	HDECA1006ECZZ	AD	N	D	Dec.panel for battery cover
4	PZETL1013ECZZ	AA	N	C	Panel insulator sheet
5	PZETL1007ECZZ	AA	N	C	Battery sheet
6	GCABB1003ECZZ	AC	N	D	Top cabinet
7	PZETL1012ECZZ	AA	N	C	Battery insulator sheet
8	QTANZ1002ECZZ	AB	N	C	Battery terminal ⊖
9	QTANZ1001ECZZ	AB	N	C	Battery terminal ⊕
10	PZETL1010ECZZ	AA	N	C	Terminal insulator sheet
11	PSLDC1010ECZZ	AB	N	C	Shield plate
12	DUNTK1048ECZZ	BP	N	E	RAM PWB unit (This includes №7~10,101~106)
13	PSHEP1011ECZZ	AB	N	C	Spring fixing sheet
14	MSPRC1202CCZZ	AC		C	Spring
15	GCABC2672CCSA	AC	N	D	Terminal cover
16	GCABA1004ECZZ	AF	N	D	Bottom cabinet
101	QSW-S1347CCZZ	AH		B	Slide switch
102	RC-SZ1007CCZZ	AF		C	Capacitor (1μF)
103	RH-DZ1008CCZZ	AC		B	Diode (DAN202)
104	VHD1SS98///-1	AD		B	Diode (1SS98)
105	VHiTC74HC139F	AH	N	B	IC (TC74HC139F)
106	VRS-TP2BD564J	AA		C	Resistor (1/8W 560KΩ ±5%)
201	GCASP1091CCZZ	AE		D	Case
202	GCASP1092CCZZ	AD		D	Case cover
203	GFTAU1281CCSA	AB	N	D	Reverse side (space)
204	PPACG1001ECZZ	AE	N	C	Module separater
205	TCAUH1002ECZZ	AB	N	C	Caution Card
206	TCAUZ1003ECZZ	AE	N	C	Caution label
207	TiNSE1036ECZZ	AU	N	D	Instruction book (USA only)
	TiNSM1037ECZZ	AR	N	D	Instruction book (E,F,G,S,I)
208	TLABZ1690CCZZ	AA		D	Switch cover label
209	UKOGD1009CCZZ	AC		C	Driver ⊕
301	SPAKA7307CCZZ	AC		D	Packing cushion
302	SPAKC0089ECZZ	AF	N	D	Packing case

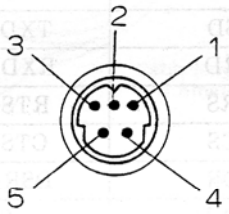


MODEL CE-1600L

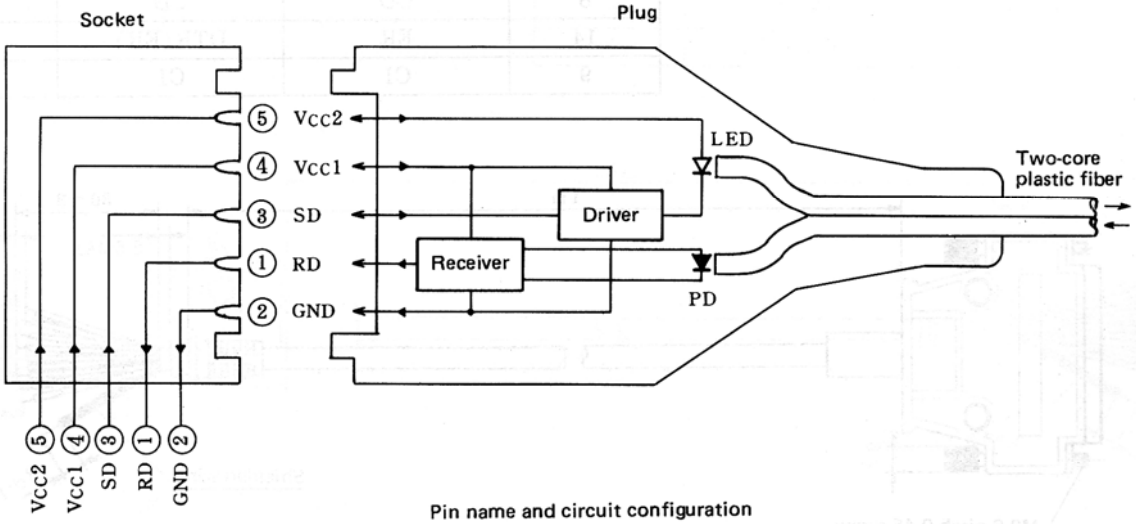
- Optical fiber cable
- No service parts is available for this product.

Appearance of cable and pin configuration





Pin No.	Signal name
1	RD
2	GND
3	SD
4	Vcc
5	Vcc

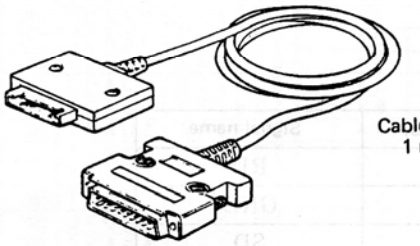


Pin name and circuit configuration

MODEL CE-1601L

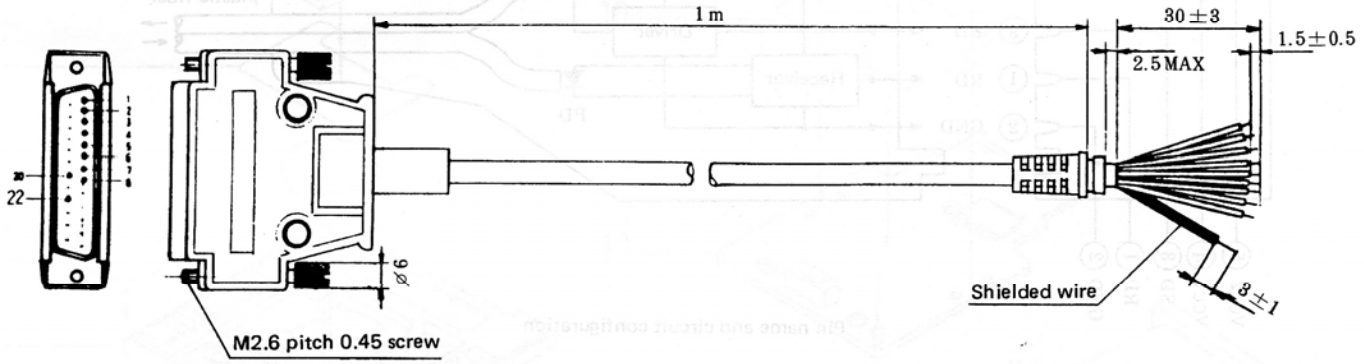
- RS-232C interface cable
- Cable used to inerface with PC-1600 and Modem unit.
- No service parts is available for this product.

Appearance of cable and pin configuration



Pin description

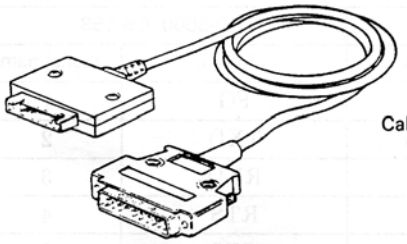
PC-1600		MODEM SIDE	
Pin No.	Signal name	Pin No.	Signal name
1	FG	FG	1
2	SD	TXD(SD)	2
3	RD	RXD(RD)	3
4	RS	RTS(RS)	4
5	CS	CTS(CS)	5
6	DR	DSR(DR)	6
7	GND	SG	7
8	CD	CD	8
14	ER	DTR(ER)	20
9	CI	CI	22



MODEL CE-1602L

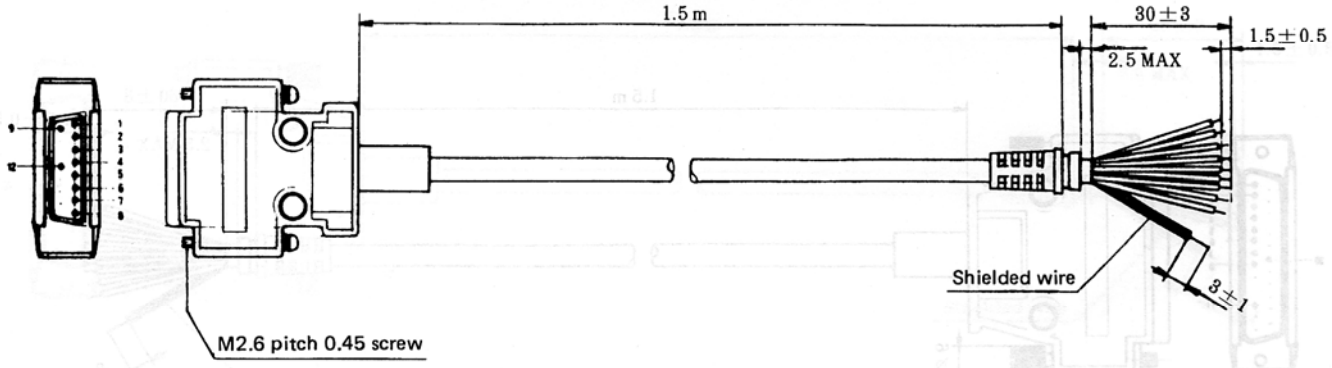
- RS-232C interface cable
- Cable used to interface with PC-1600 and the MZ-5600 (or MZ-5500).
- No service parts is available for this product.

Appearance of cable and pin configuration



Pin description

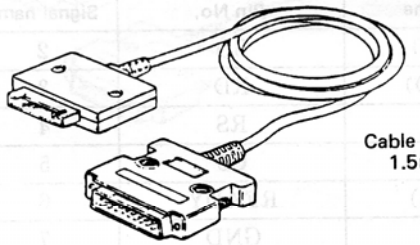
PC-1600		MZ-5600, MZ-5500	
Pin No.	Signal name	Pin No.	Signal name
3	RXD(RD)	SD	2
2	TXD(SD)	RD	3
8	CD	RS	4
4	RTS(RS)	CS	5
5	CTS(CS)	READY	6
7	SG	GND	7
14	DTR(ER)	DR	8
6	DSR(DR)	ER	12



MODEL CE-1603L

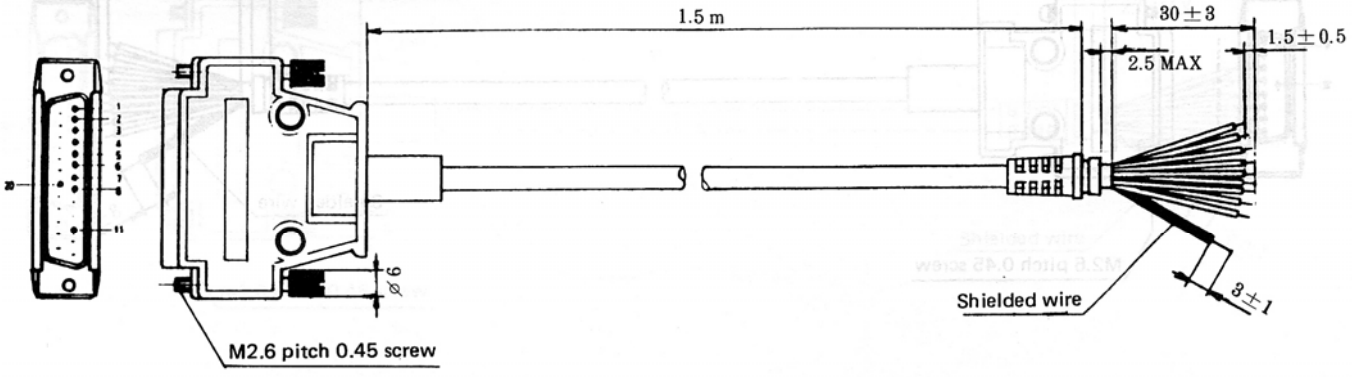
- RS-232C interface cable
- Cable used to interface with PC-1600 and the PC-5000 (or CE-158)
- No service parts is available for this product.

Appearance of cable and pin configuration



Pin description

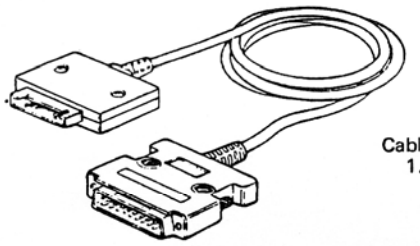
PC-1600		PC-5000, CE-158	
Pin No.	Signal name	Pin No.	Signal name
1	FG	FG	1
3	RXD(RD)	TXD	2
2	TXD(SD)	RXD	3
8	CD	RTS	4
8	CD	CTS	5
14	DTR(ER)	DSR	6
7	SG	GND	7
4	RTS(RS)	CD	8
		[RR]	11
5	CTS(CS)	DTR	20



MODEL CE-1604L

- RS-232C interface cable
- Cable used to interface with PC-1600 and the PC-7000
- No service parts is available for this product.

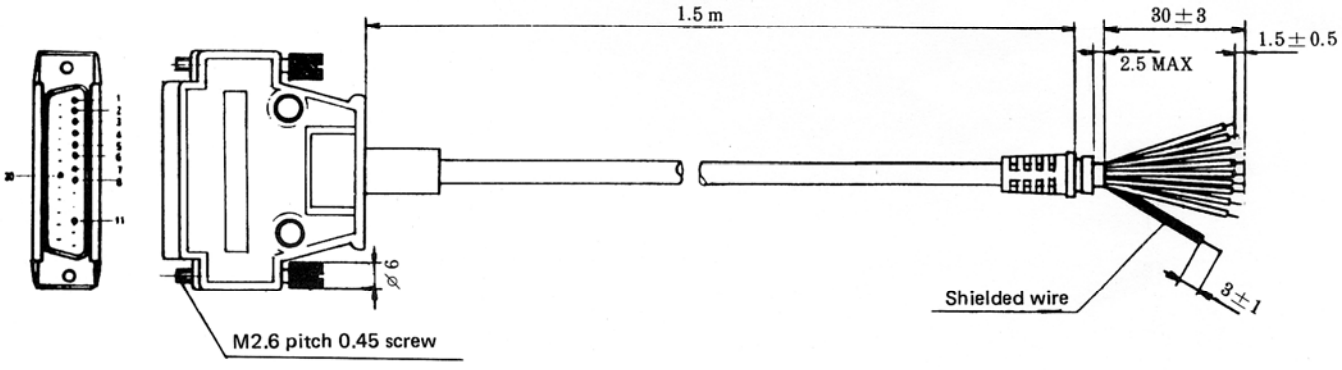
Appearance of cable and pin configuration



Cable length:
1.5meter

Pin description

PC-1600		PC-7000	
Pin No.	Signal name	Pin No.	Signal name
1	FG	FG	1
3	RD	SD	2
2	SD	RD	3
8	CD	RTS	4
8	CD	CTS	5
14	ER	DSR	6
7	SG	GND	7
4	RS	CD	8
5	CS	DTR	20
		〔CI〕	22



SHARP

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