TC8576AF TC8577AP TC8578AP

(Combination Peripheral Controller)

1. INTRODUCTION

The TC8578AP series LSI(CPC) is a single chip C-MOS LSI which has been developed to support both the RS-232C serial interface and the parallel interface based on Centronics standards.

The CPC includes the RS-232C-ART, the Baud Rate Generator for it, and the transmit/receive interface for Centronics. The Centronics interface is so designed that either a transmit mode or a receive mode may be selected.

Device No.	Package	Function
TC8576AF	44 pin miniFP	Parallel I/O user selectable
TC8577AP	40 pin DIP	Parallel output mode selected
TC8578AP	40 pin DIP	Parallel input mode selected

The ART (Asynchronous Receiver Transmitter) receives data from the CPU, and converts into serial data to transmit it from TxD terminal. Further, the ART receives serial data from the RxD terminal, and converts it into parallel data so that the CPU may receive it. Whenever the ART has sent out the data received from the CPU or whenever the ART has received data to be delivered to CPU, it can announce it to the CPU.

The XCLK input of CPC is divided by 4-bit programmable prescaler to serve as an internal CLOCK (SYS_CLK). This SYS_CLK is divided by the Baud Rate generator which is consisted of a 12-bit programmable divider. An arbitrary Baud Rate corresponding to 50 to 375000 Baud can be generated.

The parallel interface is an interface in response to the Centronics standard, which has additional pin functions for handshaking of transmit/receive combination. For the transmission mode, when the interface receives an 8 bits data from the CPU, this generates a strobe-pulse of programmed width. For the receive mode, when the interface receives external strobe, the interface response with BUSY and informs it to the CPU.

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2. FEATURES

- 8-Bit CPU Bus compatible
- Serial Interface (Asynchronous Receiver Transmitter)
  - 5 to 8 Bit characters programmable
  - 1 or 2 Stop Bits programmable
  - False Start Bit Detection
  - Automatic Break Detect and Handling
  - Full Double Buffering
  - Parity Bit Programs (NON, EVEN, ODD)
  - Error Detection (Parity, Overrun, Framing)
  - Baud Rate Generator (12 Bits programmable divider)
- Parallel interface (Based on Centronics)
  - Transmit (TC8576AF, TC8577AP)
    - PRIME output control (pulse & level)
    - Data strobe Delay and pulse width programmable
    - Interrupt generation caused by BUSY release or ACK receive
  - Receive (TC8576AF, TC8578AP)
    - Automatic generate of ACK pulse (Pulse Width programmable)
    - Busy control and interrupt generation caused by data receive
- All Inputs and Outputs are TTL Compatible (Except CDS pin of TC8576AF)
- Silicon-gate CMOS Construction
- Single -3 to 6V Supply
- 40-Pin DIP or 44-Pin mini flat Package
- I/O Port Schmitt Trigger
- Single TTL Clock (max. 10MHz @Vcc 5.0 ± 0.5V)
- (Internal Clock) (max. 6MHz @Vcc 5.0 ± 0.5V)

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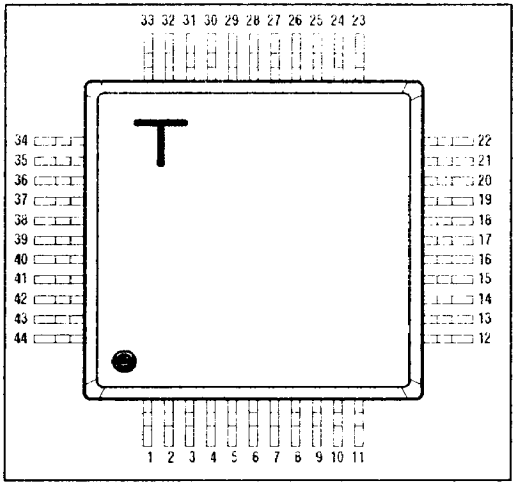
3. DESCRIPTION OF PIN

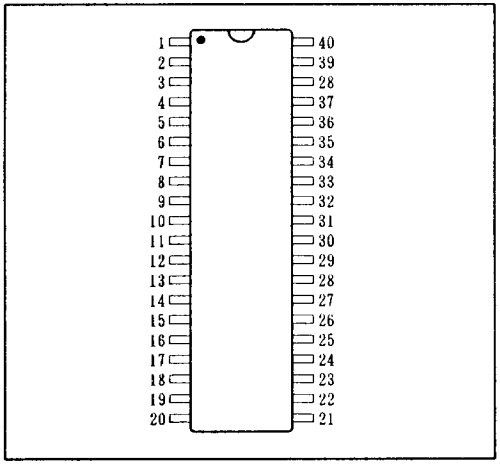
3.1 PIN ASSIGNMENT

TC8576AF



PIN NO.	I/O	PIN NAME	PIN NO.	I/O	PIN NAME
1		NC	23	I/O	/DATA5
2	I	/RD	24	I/O	/DATA6
3	I	WR	25	I/O	/DATA7
4	I	/CS	26	I/O	/DATA8
5	I	A1	27	I/O	DSTB
6	I	A0	28	I/O	ACK
7	V	GND	29	I/O	FAULT
8	O	/INT	30	I/O	/BUSY
9	I/O	DB7	31	I/O	PRIME
10	I/O	DB6	32	I/O	/SLCT
11	I/O	DB5	33	O	/RTS
12	I/O	DB4	34	I	/DSR
13	I/O	DB3	35	I	/CTS
14	I/O	DB2	36	O	DTR
15	I/O	DB1	37	O	TXD
16	I/O	DB0	38	I	RXD
17	V	VCC	39	V	VCC
18	G	GND	40	I	CDS
19	I/O	/DATA1	41	I	XCLK
20	I/O	/DATA2	42	I	/RESET
21	I/O	/DATA3	43	I/O	/P5V
22	I/O	/DATA4	44	I/O	/PE

TC8577AP, TC8578AP



PIN NO.	I/O	PIN NAME	PIN NO.	I/O	PIN NAME
1	V	VCC	21	I/O	/DATA1
2	I	XCLK	22	I/O	/DATA2
3	I	/RESET	23	I/O	/DATA3
4	I/O	/P5V	24	I/O	/DATA4
5	I/O	/PE	25	I/O	/DATA5
6	I	/RD	26	I/O	/DATA6
7	I	/WR	27	I/O	DATA7
8	I	/CS	28	I/O	DATA8
9	I	A1	29	I/O	DSTB
10	I	A0	30	I/O	ACK
11	V	GND	31	I/O	FAULT
12	O	/INT	32	I/O	/BUSY
13	I/O	DB7	33	I/O	PRIME
14	I/O	DB6	34	I/O	/SLCT
15	I/O	DB5	35	O	/RTS
16	I/O	DB4	36	I	/DSR
17	I/O	DB3	37	I	/CTS
18	I/O	DB2	38	O	/DTR
19	I/O	DB1	39	O	TXD
20	I/O	DB0	40	I	RXD

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3.2 PIN FUNCTION

o /RESET ..... Input (active LOW)
A "Low" on this input forces the CPC into "idle" mode.

o XCLK ..... Input
The XCLK is input of internal 4-bit programmable divider to genarate system clock (SYS_CLK). The SYS_CLK is used to generate internal device timing and as source signal of Baud Rate Generator. Usually the system clock (SYS_CLK) will be feed as from 400KHz to 10MHz.

o /WR (Write) ..... Input (ACTIVE LOW)
A "Low" on this input informs the CPC that the CPU is writing data or control words to the CPC.

o /RD (Read) ..... Input (ACTIVE LOW)
A "Low" on this input informs the CPC that the CPU is reading data or status information from the CPC.

o A1, A0 (Address 1,0) ..... Input
These inputs, in conjunction with the /WR and /RD inputs, informs the CPC the kind of contents on the Data Bus.

o /CS (Chip Select) ..... Input (ACTIVE LOW)
A "Low" on this input activates the CPC. When /CS is "High", /RD and /WR will have no effect on the CPC.

DATA BUS MODE

A1	A0	/RD	/WR	/CS	FUNCTION
0	0	0	1	0	RxS -> Data Bus Serial
0	0	1	0	0	Data Bus -> TxD Serial
0	1	0	1	0	PIN -> Data Bus Parallel
0	1	1	0	0	Data Bus -> POUT Parallel
1	0	0	1	0	Serial Status -> Data Bus
1	0	1	0	0	Data Bus -> Parameter Register
1	1	0	1	0	Parallel Status -> Data Bus
1	1	1	0	0	Data Bus -> Command + Parameter Address
x	x	x	x	1	Data Bus Hi-Z
x	x	1	1	0	Data Bus Hi-Z

x Don't care

o /DSR (Data Set Ready) ..... Input (For Serial)
This input is a general purpose, 1-bit inverting input terminal. It's condition can be tested checking the bit-7 in the Serial Status Register. The /DSR input is normally used to test Modem conditions such as Data Set Ready.

o /DTR (Data Terminal Ready) ..... Output (For Serial)
This output is a general purpose, 1-bit inverting output terminal. It can be set "Low" by programming "1" on the bit-1 in the Serial Command Register. The /DTR output signal is normally used for Modem control such as Data Terminal Ready.

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o /RTS (Request to Send) ..... Output (For Serial)
This output is a general purpose, 1-bit inverting output terminal. It can be set "Low" by programming "1" on the bit-5 in the Serial Command Register. The /RTS output signal is normally used for Modem control such as Request to Send.

o /CTS (Clear to Send) ..... Input (For Serial)
A "Low" on this input enables the CPC to transmit serial data if the TxEN-bit in the Serial Command Register is set "1".

o TxRDY (Transmitter Ready) ..... Internal signal (For Serial)
This status bit signals the CPU that the serial transmitter is ready to accept a data character. This signal is set "High" when the data receive buffer is empty and transmit is enable (TxEN=1).

o RxRDY (Receiver Ready) ..... Internal signal (For Serial)
A "High" on this signal means the ART has a character to transfer the CPU. The RxRDY signal is logical ORed with the TxRDY (mentioned above) and lead on to INT out terminal.
This content is same as the bit-1 in the Serial Status Register. The RxRDY is automatically reset when the CPU read the character.

o TxD (Transmitter Data) ..... Output (For Serial)
The TxD is output terminal to transmit the serial data.

o RxD (Receiver Data) ..... Input (For Serial)
The RxD is input terminal to receive the serial data.

o INT (Interrupt) ..... Output [ACTIVE HIGH (For General)]
The INT output is a logical ORed of four internal signal, that is, RxRDY, TxRDY, PRRDY and PTRDY, so as to use as a interrupt acknowledge signal of the CPU.

o CDS (Centronics Direction Select) ..... Input
The CDS is input to select a direction of the parallel interface. When CDS is GND level(CDS=0), parallel interface block is defined as parallel output mode. When CDS is VCC level(CDS=1), parallel interface block is defined as parallel input mode.
(TC8577AP/TC8578AP is already connected "GND"/"VCC" respectively.)

o /DATA1 to /DATA8 (Data Bus) ..... Input/Output (For Parallel)
The /DATA8-1 are the 8-bits data bus for parallel interface.
(CDS=1): The /DATA8-1 work as parallel input port.
(CDS=0): The /DATA8-1 work as parallel output port.
The content of Data Bus is inverted.

o ACK (Acknowledge) ..... Output/Input (For Parallel)
(CDS=1): The ACK output issues the ACK signal. Its pulse width are programmable.
(CDS=0): The ACK input receives the ACK signal to reset the internal Xbusy signal.

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o DSTB (Data Storobe) ..... Input/Output (For Parallel)
(CDS=1): The DSTB input is storobe signal to catch the data on the parallel port.
(CDS=0): The DSTB output is storobe signal to indicate that the parallel output data is valid. Its pulse dalay and width are programable.

o /BUSY (Busy Signal) ..... Output/Input (For Parallel)
(CDS=1): The /BUSY output issues the Busy signal which is set by catching a data from the parallel port.
(CDS=0): The /BUSY input senses the Busy status of external device.

o /SLCT (Select) ..... Output/Input (For Parallel)
(CDS=1): The /SLCT is inverted output to issues the content of the bit-1 on the Parallel Command Register.
(CDS=0): The /SLCT input senses the select Status of external device.
The SLCT is normally used for detect/announce the device select status.

o FAULT (Fault Signal) ..... Output/Input (For parallel)
(CDS=1): The Fault output issues the content of the bit-0 on the Parallel Command Register.
(CDS=0): The Fault input senses the Fault status of the external device.
The FAULT is normally used for detect/announce the device fault.

o PRIME (PRIME) ..... Input/Output (For Parallel)
(CDS=1): The PRIME is an 1-bit input terminal.
(CDS=0): The PRIME output issues the PRIME signal, it can be programmed it's mode (level ON, level OFF, one-shot).

o /P5V (Plus 5 Volt) ..... Output/Input (For Parallel)
(CDS=1): The /P5V is an inverted output to issues the content of the bit-3 on the Parallel Command Register.
(CDS=0): The /P5V is an inverted input to sense the power supplying status of the external device.

o /PE (Paper End) ..... Output/Input (For Parallel)
(CDS=1): The /PE is an inverted output to issues the content of the bit-2 on the Parallel Command Register. inverted output terminal.
(CDS=0): The /PE is an inverted input to sense the Paper End signal of the external device.

o PRRDY (Parallel Receiver Ready) ..... Internal signal
A "High" on the PRRDY indicate that the parallel interface has a character to be sent to the CPU.

o PTRDY (Parallel Transmitter Ready) ..... Internal signal
A "High" on the PTRDY indicate that the parallel interface can be receive a Data from CPU.

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4. INTERNAL REGISTER

Register name (R:/RD=0, W:/WR=0)		A1	A0	D7	D6	D5	D4	D3	D2	D1	D0	Shows hardware reset Meaning	
Serial input data register	R	0	0	D7	D6	D5	D4	D3	D2	D1	D0	Serial input data byte	
Serial output data register	W	0	0	D7	D6	D5	D4	D3	D2	D1	D0	Serial output data byte	
Parallel input data register	R	0	1	D7	D6	D5	D4	D3	D2	D1	D0	Parallel port input data byte	
Parallel output data register	W	0	1	D7	D6	D5	D4	D3	D2	D1	D0	parallel port output data byte	
0	W	1	0	B7	B6	B5	B4	B3	B2	B1	B0	Baud Rate Low	
Parameter register 1	W	1	0	x	x	x	x	B11	B10	B9	B8	Baud Rate High	
Parameter register 2	W	1	0	x	x	x	DL4	DL3	DL2	DL1	DL0	DSTB delay/ACK width	
3	W	1	0	x	x	x	W4	W3	W2	W1	W0	DSTB width	
4	W	1	0	x	x	SR5	SR4	SR3	SR2	SR1	SR0	PRIME length	
5	W	1	0	RxM	ERM	EP	PEN	L2	L1	TxM	S0	Serial mode	
6	W	1	0	x	x	x	x	x	x	PP1	PP0	Parallel mode	
7	W	1	0	x	x	x	x	K3	K2	K1	K0	Prescaler value	
Serial status register	R	1	0	DSR	RBRK	FE	OE	PE	Tx EMP	Rx RDY	Tx RDY	Serial I/O status byte	*
Serial command register	W	1	1	0	x	RTS	ERS	SBRK	RxEN	DTR	TxEN	Serial I/O command byte	*
parallel command reg.	W	1	1	1	0	IM1	IM2	x	S2	S1	S0	CDS=0:output mode CDS=1:input mode	*
						IM	(a)	P5V	PE	SLCT	FALT		
Parameter address reg.	W	1	1	1	1	re-set	x	x	PR2	PR1	PR0	System reset bit & Parameter address	
Parallel status reg.	R	1	1	IntF	(b)	BUSY	PRIM	P5V	PE	SLCT	FALT	Parallel I/O status byte	*

Note: (a) Busy on (b) XBUSY/BUFFUL x Don't care

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4.1 Selection of Parameter Register

At the write operation on the condition that both A1 and A0 are "1" (A1=1,A0=1,/CS=1,/WR=1,/RD=0), the one of three registers by the contents of D7 and D6 as follows.

Serial Command Register

D7	D6	D5	D4	D3	D2	D1	D0
0	<----- Command byte ---------->						

The 7-bits word will be used for serial interface as a command.

Parallel Command Register

D7	D6	D5	D4	D3	D2	D1	D0
1	0	<----- Command byte ----->					

The 6-bits word will be used for parallel interface as a command.

Parameter Address Set Register

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1/0	X	X	PA2	PA1	PA0

-- The 3-bits(D2-D0) point to an address of the Parameter Register(PR0-PR7).

An "1" on this bit will cause the system reset same as external reset.

4.2 Parameter Register (A1=1,A0=0,/CS=0,/WR=0,/RD=1)

One of eight Parameter Registers(PR0-PR7) is selected by the Parameter Address Set Register(A1=1,A0=1,D7=1,D6=1). the address of each Parameter Register is shown in follows.

Internal Parameter Register

Register Address			Register Name	Corresponding Bit							
				7	6	5	4	3	2	1	0
PR0	0	0 0	Baud divider BL	B7	B6	B5	B4	B3	B2	B1	B0
PR1	0	0 1	Baud divider BH	x	x	x	x	B11	B10	B9	B8
PR2	0	1 0	Delay time	x	x	x	D4	D3	D2	D1	D0
PR3	0	1 1	Pulse width	x	x	x	W4	W3	W2	W1	W0
PR4	1	0 0	PRIME timer	x	x	SR5	SR4	SR3	SR2	SR1	SR0
PR5	1	0 1	Serial mode	Rx INTM	ER INTM	EP	PEN	L2	L1	Tx INTM	SO
PR6	1	1 0	Parallel mode	x	x	x	x	x	x	P1	P0
PR7	1	1 1	Prescaler value	x	x	x	x	K3	K2	K1	K0

x Don't care

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4.3 Prescaler and Internal clock

The CPC has a 4-bits prescaler to divide the external clock (XCLK) into the internal clock (SYS_CLK). Therefore, the CPC can be feed a clock whose frequency is from 400KHz to 10MHz.

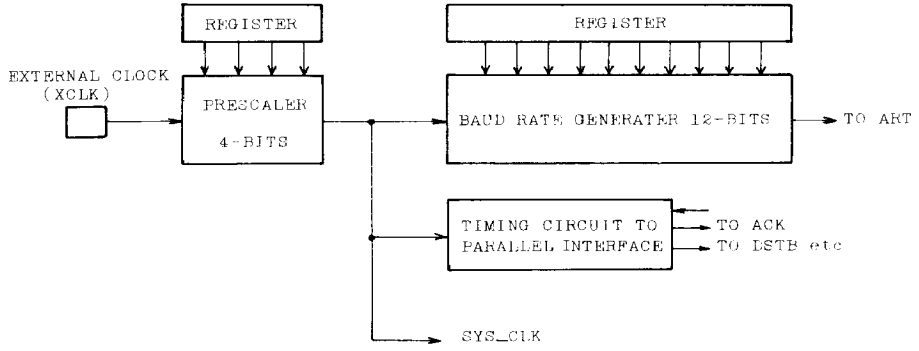

Fig. 4.3 Internal Clock Circuit Block Diagram

The value of prescaling factor is assigned on the LSB portion of the Parameter Register(PR7). The relation between the value of PR7 and prescaling operation is as follows.

Prescalar value (PR7)

D7	D6	D5	D4	D3	D2	D1	D0
x	x	x	x	K3	K2	K1	K0

x Don't care

: assuming the value of K as follows

$$K = 8 \times K3 + 4 \times K2 + 2 \times K1 + K0$$

then

	fSYS_CLK	Pulse duty of fSYS_CLK
K = 0	fXCLK/16	1/16
K = 1	fXCLK	same as XCLK
2 < K < 15	fXCLK	1/K

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4.4 Baud Rate Generator (PR0,PR1)

To generate a source clock for asynchronous serial channel, the CPC has a 12-bits programmable divider. The value of divisor is assigned parameter register PR1 and PR0 into two parts i.e. MSB 4 bits and LSB 8 bits respectively as follows.

PR1								PR0							
D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
x	x	x	x	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0

x Don't care

The frequency of the Baud Rate Generator and the value of divisor on PR1 and PR0 is as follows.

Assuming that

$B = 2048 \times B11 + 1024 \times B10 + \ldots + 2 \times B1 + B0$

B = 0	fBaud8x = fSYS CLK/4096
B = 1	fBaud8x = 0 (no operation)
2 < B < 4095	fBaud8x = fSYS CLK/B

Asynchronous channel needs eight times clock frequency for producing real Baud Rate, so we call the output of Baud Rate Generator as Baud8x.
Final Baud Rate depends on the value of fXCLK, prescaler and Baud Rate divider. And also there are some limitation of chosing these values, so that the SYS_CLK is already used by another circuit for time base. Next tables show some example using an 8MHz (7,987,200Hz) XCLK or a 6MHz (6,144,000Hz) XCLK.

fXCLK = 6 MHz (6,144,000 Hz)

Prescaler value		1	4	5
fSYS CLK (Hz)		6,144,000	1,536,000	1,228,800
Parallel interface	resolution	0.162 uS	0.651 uS	0.814 uS
	Pulse width max. (DSTB, ACK)	5.3 uS	21.5 uS	26.9 uS
	Pulse width max. (PRIME)	10.7 uS	42.3 uS	52.9 uS
The value of B for corresponding Baud Rate	110	= 6982	= 1745	= 1396
	75	10240	2560	2048
	150	5120	1280	1024
	300	2560	640	512
	600	1280	320	256
	1200	640	160	128
	2400	320	80	64
	4800	160	40	32
	9600	80	20	16
	19200	40	10	8
	38400	20	5	4
	76800	10		2
	153600	5		

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fXCLK = 8 MHz (7,987,200 Hz)

Prescaler value		4	8	13
fSYS CLK (Hz)		1,996,800	998,400	614,400
Parallel interface	minimum unit	0.5 uS	1 uS	1.63 uS
	Pulse width max. (DSTB) ACK	16.5 uS	33 uS	52.8 uS
	Pulse width max. (PRIME)	33 uS	66 uS	105.6 uS
The value of B for corres ponding Baud Rate	110	= 2269	= 1135	= 698
	75	3328	1664	1024
	150	1664	832	512
	300	832	416	256
	600	416	208	128
	1200	208	104	64
	2400	104	52	32
	4800	52	26	16
	9600	26	13	8
	19200	13	-	4
	38400	-	-	2

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4.5 System reset and Initialization

The CPC will be initialized when the RESET(external terminal) is "Low" level, and also when an "1" is programmed on a Bit-5 of the Parameter Address Set Resister. By above operation, the System Reset FF(internal flip flop) is set and sustain this condition until a "0" is programmed on a Bit 5 of the Parameter Address Set Register.
This is useful to suppress desirable spurious whole the time when the power supply goes up and till the initialize program sets the all parameter precisely.

The result of system reset appears in some internal registers (shown in Internal Register Table as * marked) and in some internal status.
Register initializing is shown as follow.

	D7	D6	D5	D4	D3	D2	D1	D0
Serial status	DSR	RBRK	FE	OE	PE	TxEMP	RxRDY	TxRDY
Value	external	0	0	0	0	1	0	TxIMTM
Serial command	0	-	RTS	ERS	SBRK	RXEN	DTR	TxEN
Value		-	0	(1)	0	0	0	0
Parallel command	1	0	IM1	IM2	x	S2	S1	S0
			IM	Busy on	P5V	PE	SLCT	FAULT
Value			1	1	0	0	0	0
Parallel status	Intr flag	XBUSY/ BUFUL	BUSY	PRIM	P5V	PE	SLCT	FAULT
Value of Output (CDS = 0)	0	0	exit	0	exit	exit	exit	exit
Value of Input (CDS = 1)	0	0	1	exit	0	0	0	0

Other internal states is shown below.

Prescaler and Baud Rate Gen.	As the CLK input is applied, these circuits are running. There are no changes by initialization. The dividing counter will be initialized only the new value is applied on its divisor register at the parameter set operation.
Timing circuit for ACK, DSTB and PRIME	By initialization, the circuit is reset, but register values are not change.
BUSY output (CDS=1)	The /BUSY output will be active. (Low level)
TXD terminal	TxD goes to High level. The initialization resets the transmitter directly whole circuit, so that even if in a transmitting sequence, it will be stopped.
Serial receiver	The RxEN reset to no-active ("0"). All internal flags inclusing of Error is reset.

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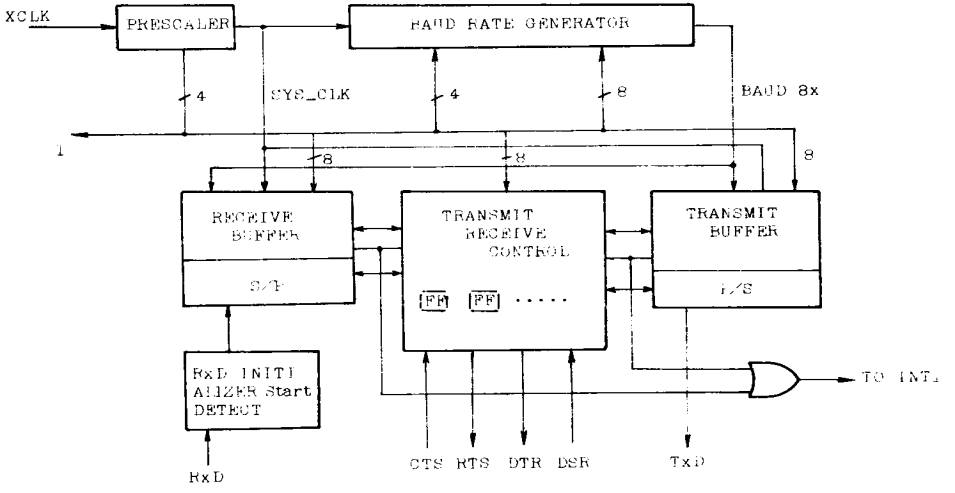
5. SERIAL INTERFACE

5.1 Block Diagram of Serial Interface



The RxD initialization circuit reserves the start-bit detection until valid "1" is appeared on RXD after reset. It prevents a mistaken break signal detection for the unused line. Its valid "1" detection means detecting two continues "1" at each sampling by the Baud8x clock.
In addition, this circuit gets active immediately after a break detection. This function prevents a mistaken character reception of "0" level at the end point of break signal as receiving character, which is not as long as one character length. In this case, the valid "1" is detected by one time sampling of Baud8x clock.

When the transmitter has a character to be sent, validity of CTS on(CTS=1) and TxEN on(TxEN=1) and TxRDY(Transmit ready) is evaluated on each Baud8x clock cycle before starting transmit. When CTS or TxEN is off, the transmitter is disable transmittion condition.

5.2 Programming of Serial Channel

Before starting Transmittion or Reception of the Data, the CPU must program the parameters and the command of the CPC. The serial operation is defined by these values.
The contents of parameter registers should be filled by the values which is needed to open the serial channel. Concerning about Baud Rate, it must be programmed to supply a clock which has 8 times frequency of Baud Rate on the RxD and the TxD. (See Section 4.)
The command is programed by the byte transfer or block transfer for controlling the DTR and RTS and reseting the ERRORs.

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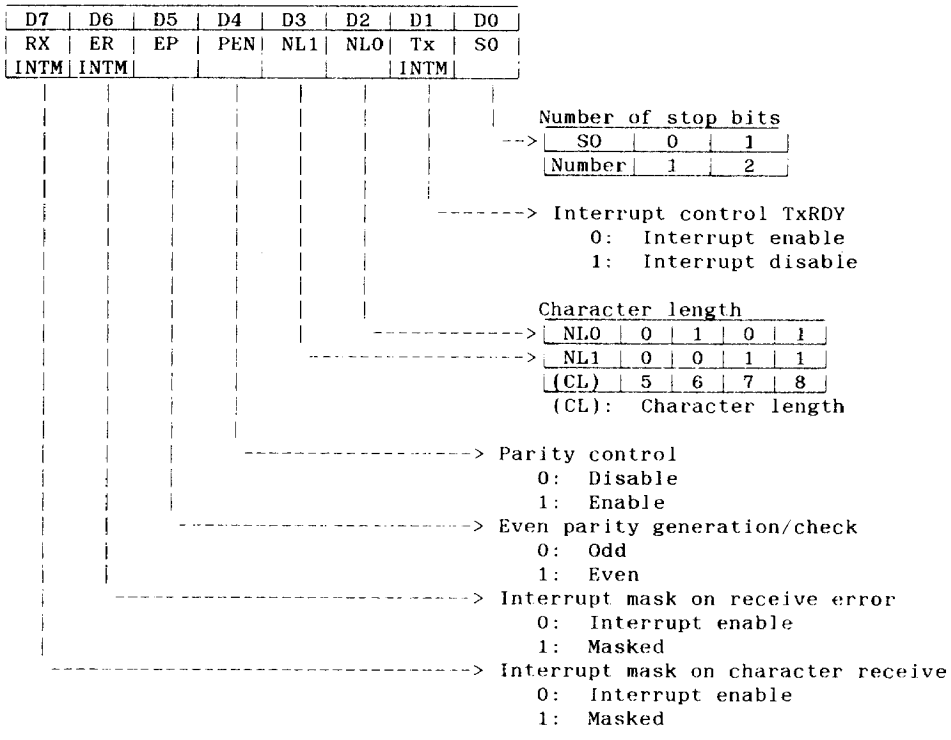
5.3 Serial Parameter Register (PR5)

The serial parameter is assigned on the parameter register PR5, and the contents have meanings as follows.



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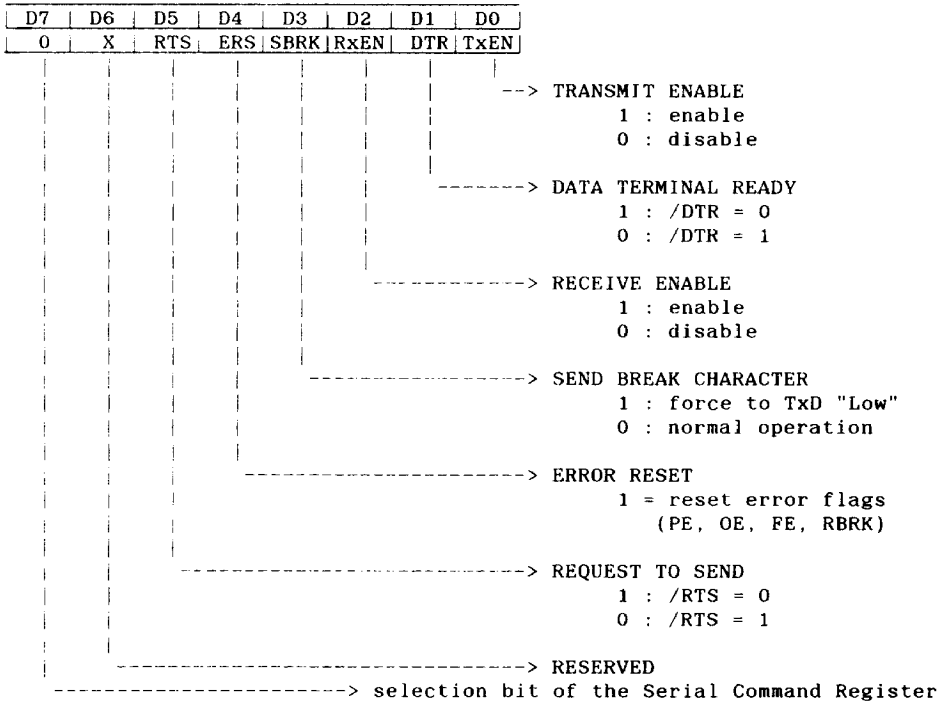
5.4 Serial Command Register (A1=1,A0=1,D7=0)

The Serial Command Register is defined as a 8-bits word which has "0" on Bit 7 and which was written by the CPU at the condition that a "High" is applied on the A1 and A0. The contents have meanings as follows.



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5.5 Serial Status Register (A1=1,A0=0)

The status of serial channel is a result of read operation with A1=0 and A0=0, and it contents have meanings as follows.

D7	D6	D5	D4	D3	D2	D1	D0
DSR	RBRK	FE	OE	PERR	TxE	Rx RDY	Tx RDY

TxRDY (Transmit Ready)

TxRDY status bit meaning changes itself depend on the value of TxINT

TxINTM = 1 (disable interrupt)

TxRDY = (Transmit Buffer is empty)

TxINTM = 0 (enable interrupt)

TxRDY = (Transmit Buffer is empty) x (/CTS = 0) x (TxEN = 1)

(This is equal to interrupt condition)

TxE (Transmit Empty)

An "1" on this bit indicates both the Buffer empty (Transmitter Buffer is empty) and off Transmittion (transmittion is not in operation).

RxRDY (Receive Ready)

An "1" on this bit indicates that the Receiver Buffer has a character which is ready to be read by CPU.

PERR (Parity Error)

The PERR bit is set when a parity error is detected.

OE (Over run error)

The OE bit is set when a previous character is lost without being read by the CPU by having received new character.

FE (Framing Error)

The FE bit is set when a valid Stop bit is not detected at the end of the character.

RBRK (Receive Break detect)

The RBRK bit is set when the receiver detect "Break condition".

DSR (Data Set Ready)

The DSR bit means inverted value of external /DSR terminal.

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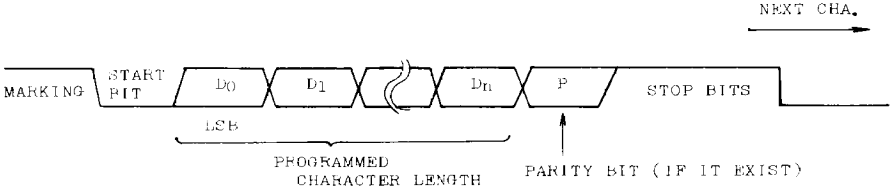
5.6 Format of data character

The RxD line and the TxD line are normally High.
Transmitter automatically adds a Start bit (low level) followed by the data bits (least significant bit first). And the programmed number of Stop bit(s) is added on tail, after a parity bit (if it is programmed) is inserted.



5.7 Data Transmittion

Upon receipt of the character, which is serial output data, from the CPU, the CPC changes to Buffer not Empty(Transmitter Buffer is not empty) at the same time evaluates TxEN(a command bit), CTS(content of /CTS terminal), and on/off-Transmittion(whether the transmitter is in operation). If the transmitter is in the condition of TxEN on, CTS on(/CTS=0), and off-Transmittion(the transmitter is not in operation), the transmit controller is transferred into the following state by the falling edge of the Baud8x clock.

The transmitter starts transmittion of the character. The transmittion of the start bit changes the state into the Buffer Empty and on-Transmittion(the transmitter is in operation). The Buffer Empty indicates that the setting a character to the Transmitter Buffer (writing to the Serial output data register) is possible.

The setting of next character changes the state into Buffer not Empty. This new character is held in the Transmitter Buffer during the on-Transmittion of the previous character. And after the stop bit(s) of the previous character has been transmitted, the transmittion of new character starts continuously. Then, the TxE (Transmit Empty) is set to "1", after all characters have been transmitted.

Even if either CTS off or TxEN off condition (which is disable transmittion condition) occurs while the transmittion is in operation, the character as whole parts including Parity and Stop bit will be sent. If a character is in the Transmitter Buffer after occurring of the disable transmittion condition, its character will be transmitted following both CTS on and TxEN on condition.

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5.8 Data Receive

The RxD line is normally High. A falling edge on this line triggers the beginning of a Start bit. The validity of this Start bit is checked by continuous four times strobing on each falling edge of the Baud8x. If four times Low is detected perfectly, the receiver regards it as a valid Start bit, and locates the center of the data bits followed and strobes those.

If the parity exist, the circuit compares the strobed parity bit with the generated parity bit by means of received data. If the comparison fails, the Parity Error flag is set.

The receiver detects only one stop bit, regardless of the programed number of stop bit(s). If a low level is detected at that point, the Framing Error flag will be set.

When the programed number of data bits are strobed, these are loaded into the Receive Buffer, and the RxRDY flag is set to "1". In this case, the non-used upper bits are automatically reset to "0".

The RxRDY flag shows that the Receive Buffer has a character which is ready to be fetched by the CPU. If a previous character has not been fetched by the CPU until the present character replaces it in the Receive Buffer, the Overrun Error Flag is set and the previous character is lost.

If the RxD line remains Low as long as double length of character including data bits, parity bit (if it exist) and stop bit(s), the receiver sets the Break detection Flag. In this case the RxD initializing circuit is activated and the Start bit detection is reserved until the "1" occurs in the RxD line.

All of the Error Flag and the Break detection flag can be reset by setting of the ERS bit in the Serial Command Register. The occurrence of any of these errors will not effect the operation of the CPC.

5.9 Interrupt Control

There are those interrupt factors in the serial channel, as follows.

1. The serial transmitter turns being able to receive a new data from the CPU.
2. The serial receiver has a character ready to send the CPU or has detected Break character.
3. The serial receiver has the Error Flag(s).

These factors can be masked or enabled to lead into INT terminal through into TxRDY and RxRDY.

$$\text{Tx interrupt} = (\text{TxEN}=1) \times (/\text{CTS}=0) \times (\text{Transmit Buffer empty}) \times (\text{TxINTM}=0)$$
$$= \text{TxRDY (in TxINTM=0)}$$
$$\text{Rx interrupt} = (\text{RxEN}=1) \times [(\text{RxINTM}=0) \times \{(\text{RxRDY}=1)+(\text{RBRK}=1)\} + (\text{ERINTM}=0)\times(\text{FE}+\text{OE}+\text{PERR})]$$

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6. PARALLEL INTERFACE [1] - OUTPUT MODE (TC8577AP,TC8576AF)

6.1 Parallel Output Interface (CDS=0)

If the CDS terminal are at the "0" level a parallel output interface is formed. An example of external circuit in this case is shown in Fig. 6.1.

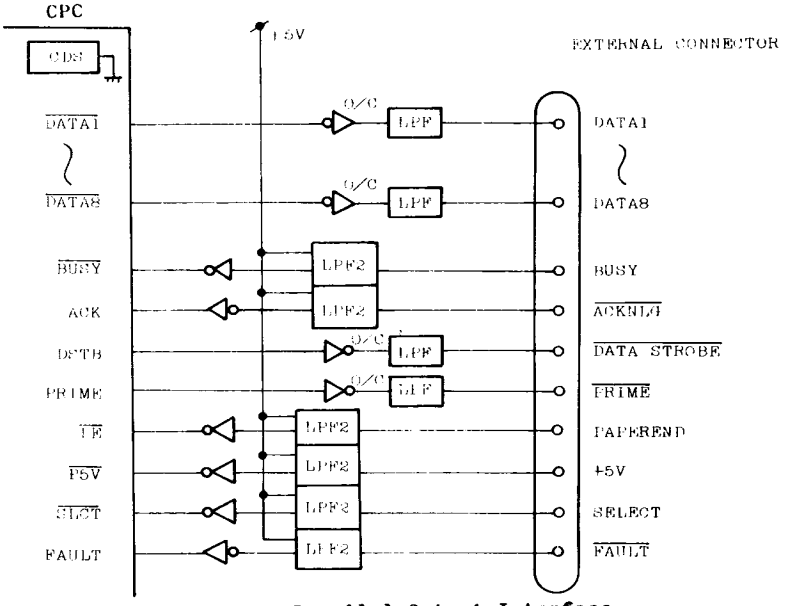
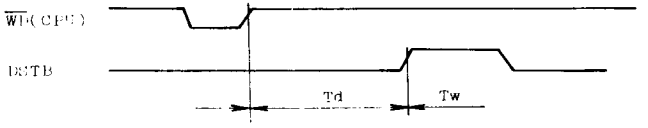


Fig. 6.1 Parallel Output Interface

6.2 Output mode operation

When the CPC receives data from the CPU, the data is output inversely on the /DATA1 to /DATA8 terminal, and the CPC automatically generates the Data Strobe(DSTB) pulse.

The characteristic of DSTB pulse is decided by both of the value set to the parameter register (PR2, PR3) and the internal SYS_CLK cycle.



Here, let the values set to the parameter register (PR2,PR3) be NSD and NSW, respectively, and conceive that TSYS = 1/SYS_CLK and x = 0 to 1, then

$$Td = TSYS \times (NSD + 2 + x)$$
$$Tw = TSYS \times (NSW + 1)$$

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In the output mode, the XBUSY flag bit fills the delay time of the external BUSY signal. The XBUSY flag is set at the rise of /WR and reset by external ACK. These timing are shown in Fig. 6.2.

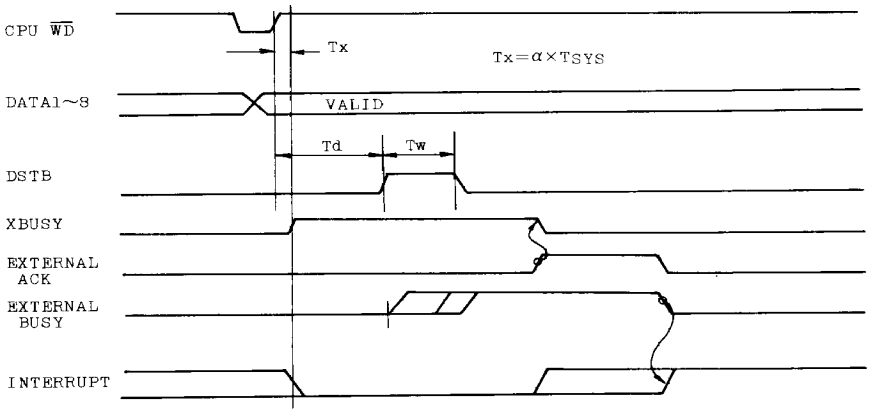

Fig. 6.2 Output Mode Timing
(In case where external BUSY includes ACK)

6.3 Parallel Status Register (A1=1,A0=1) --- Read

In the Output Mode, the Parallel Status Register has the status bits as follows.

D7	D6	D5	D4	D3	D2	D1	D0
IntF	XBUSY	BUSY	PRIM	P5V	PE	SLCT	FAULT

--> Contents of FAULT input
--------> Contents of SLCT input
-------------> Contents of PE input
-------------------> Contents of P5V input
-----------------------> Contents of PRIME output
----------------------------> Contents of BUSY input
---------------------------------> Contents of XBUSY flag
-----------------------------------> Parallel Interrupt flag

: If there are interrupt factors in parallel, the flag goes to "1".

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6.4 Parallel Command Register (A1=1,A0=1,D7=1,D6=0) --- Write

D7	D6	D5	D4	D3	D2	D1	D0
1	0	IM1	IM2	x	S2	S1	S0

----------> The following operation are performed according to a combination of S2,S1,S0.

S2	S1	S0	No.	Operation
0	0	0	0	Resetting of FAULT detection bit
0	0	1	1	Resetting of SLCT detection bit
0	1	0	2	Resetting of PE detection bit
0	1	1	3	Resetting of P5V detection bit
1	0	0	4	Level On of PRIME output
1	0	1	5	One-shot of PRIME output
1	1	0	6	Level OFF of PRIME output and resetting of all the flags including XBUSY as well as interrupt bit.
1	1	1	7	NOP (No operation)

---> Interrupt factor 2 is masked by "1".
---------> Interrupt factor 1 is masked by "1".
----------> These are bits to select the Parallel Command Register.

The commands No.0 to No.3 are used for separate resets of each detection Flag in the CPC. The commands 4 to 6 control the PRIME output.
When the command 5 is issued, the one-shot pulse is provided to the PRIME output. Its pulse width based on the value of the parameter register PR4. Once the command No.4 is issued, the PRIME output is held at the High level until the command No.5 or No.6 is issued.
The one-shot pulse width for the value of PR4 is provided by the following equation:

$$tPRIME = tSYS \times (PR4 + 2)$$

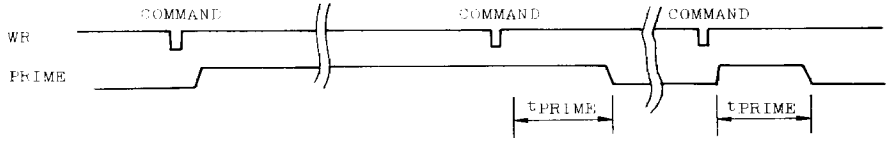

Fig. 6.4 PRIME Timing

6.5 Parallel Mode Register (PR6)

The Parameter Register PR6 is a parallel mode register, and the parallel output mode has the following bits.

D7	D6	D5	D4	D3	D2	D1	D0
x	x	x	x	x	x	PP1	PP0

-> 1:Interrupt enable at rising edge of XBUSY.
-> 1:Interrupt enable at rising edge of external BUSY.

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6.6 Flag and Interrupt control

The parallel output mode has the interrupt factors of two systems. These factors are the factor 1 which announces the response of the companion device, and the factor 2 which announces the change in the status (FAULT, +5V, SLCT, PE) of the companion device.

Interrupt factor 1:

For the interrupt factor 1, the XBUSY, the BUSY(inverse of /BUSY input) and the data Write strobe to the Parallel Output Data Register are evaluated. Herein, the two interrupt detection flags of INPT1 and INPT0 exist. INTP1_flag is set at the falling edge of BUSY. The INTP0_flag is set at the falling edge of XBUSY.

Since the XBUSY is reset at the rising edge of external ACK signal, the INTP0 is set at the rising edge of external ACK signal.

The PP1 and PP0 in the Parallel Mode Register(PR6) enable/disable (1:enable, 0:disable) the outputs of these INTP1_flag and INTP0_flag, but have no effect on the value of these flags.
Further, if D5 of parallel command word is programmed to "1", these Flags are regularly forced to the reset state, and are also reset by wiring to the Parallel Output Register or by issuing parallel command. (Data contents don't care.)

Interrupt factor 2:

The interrupt factor 2 is generated by the change in the status of the external device. Four internal interrupt flags exist in, and these contents are logical ORed to form the interrupt factor 2.

When D4 bit of the Parallel Command Register is set to "1", this interrupt factor 2 is masked without being reset of these flags. These flags are reset by the selection reset (operation code No.0 to No.3 of the Parallel Command Register) or the batch reset (operation code No.6) in addition to the master reset.

There is no essential difference in set condition among flags, excepting the difference in set condition based on the rising edge or falling edge of status signal.

The detection flag of PE(Paper End) is set at the falling edge of the /PE terminal. And the detection flags of the others (FAULT,SLCT,P5V) are set at the rising edge of each own input terminal (FAULT,/SLCT,/P5V).

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7. PARALLEL INTERFACE [2] - INPUT MODE (TC8578AP TC8576AF)

7.1 Parallel Input Interface (CDS=1)

If the CDS terminal are at the High level, a parallel input interface is formed. An example of external circuit in this case is shown in Fig. 7.1.

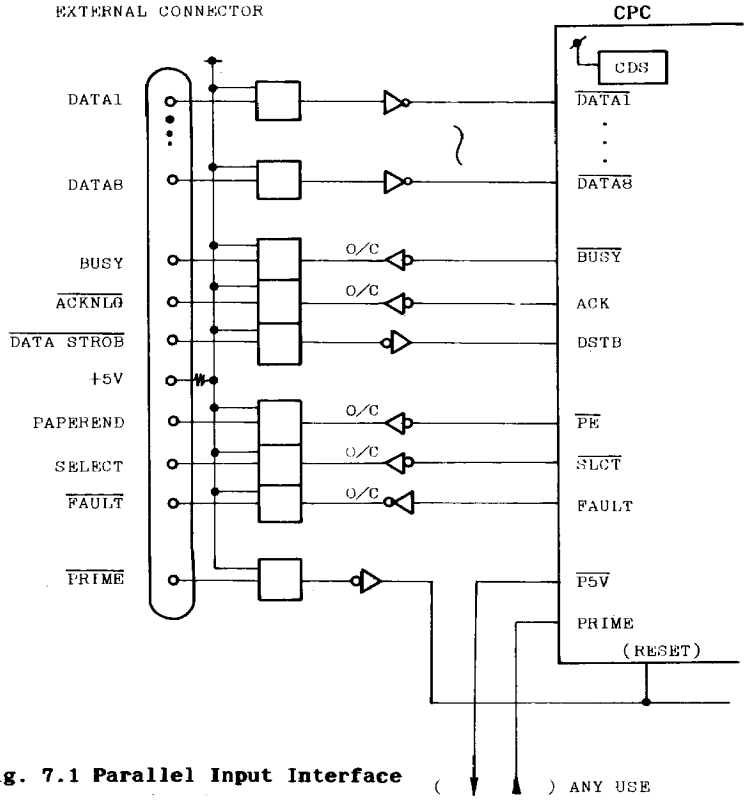

Fig. 7.1 Parallel Input Interface

7.2 Input mode operation

As soon as the CPC receives the DSTB (Data Strobe) from the outside, it forces the BUSY signal to go to the High level and announces the fact to the CPU.
The contents of DATA1 to DATA8 (inverse of /DATA1 to /DATA8) are held in the internal latch by means of the raising edge of the DSTB, and can be read by the CPU.
The timing of the BUSY reset and ACK generation can be selected either under the Read operation or the Write operation (DUMMY WRITE) by programming PP1 (D1 bit) of the Parallel Mode Register (PR6).
Further, whether ACK signal include in BUSY signal or not is decided by programming the PP0 (D0 bit) of the Parallel Mode Register (PR6).

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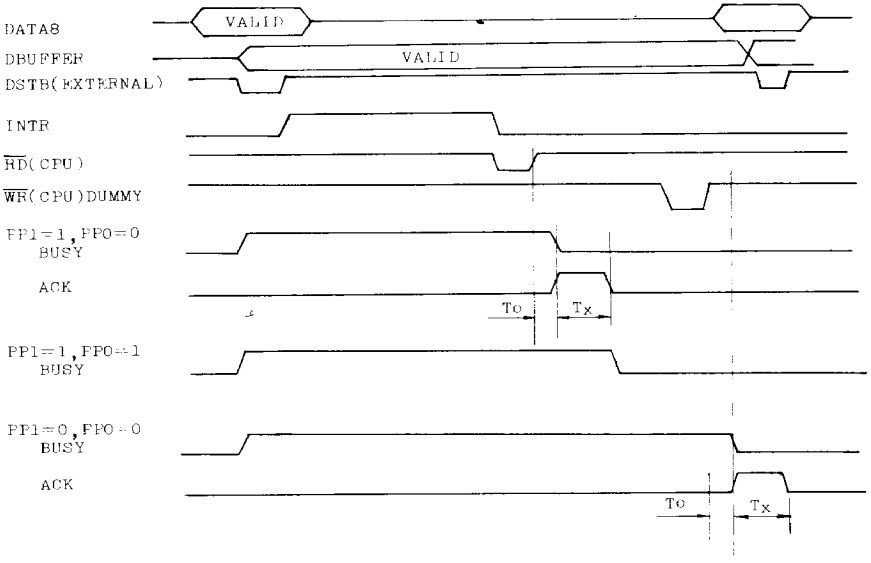

Fig. 7.2(a) Input Mode Timing

The ACK pulse is triggered at the rising edge of /RD or /WR signal from the CPU, and generated at the timing shown in Fig. 7.2(b). When the cycle of system clock (SYS_CLK) formed being divided by the prescaler is considered to be TSYS, the time To and Tw are as follows:

$$To = TSYS \times (1 + x) \quad (x = 0 \text{ to } 1)$$
$$Tw = TSYS \times (PR2 + 1)$$

The /BUSY is released at the edge of ACK pulse.

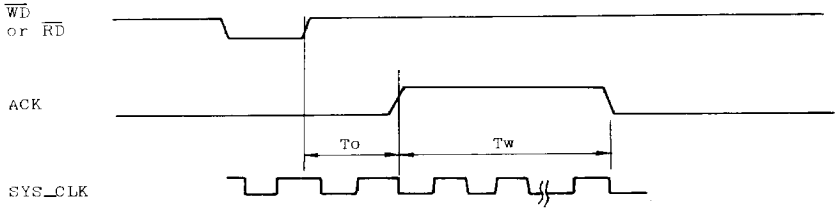

Fig. 7.2(b) ACK Pulse Timing

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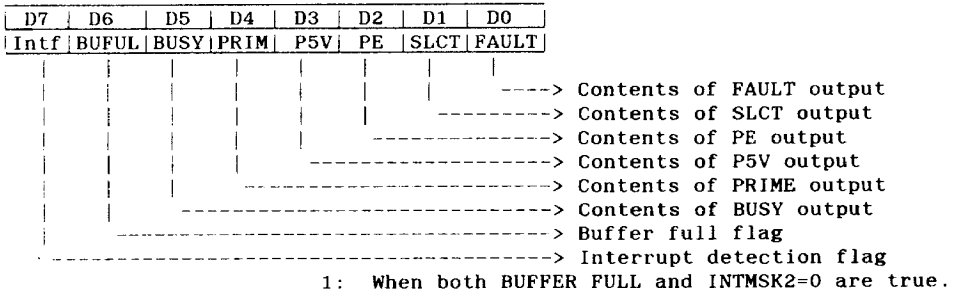
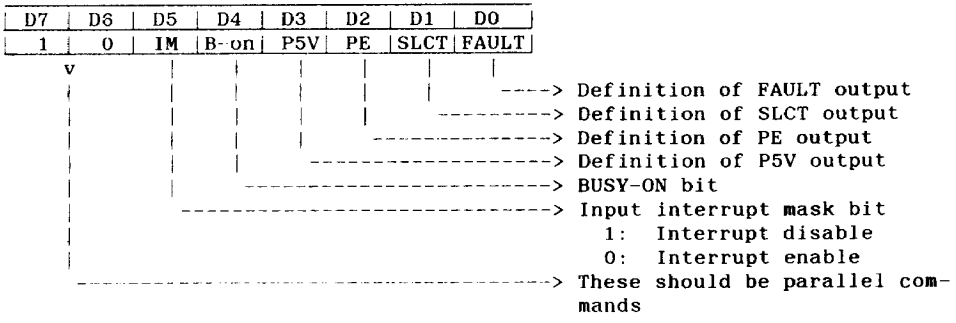
7.3 Parallel Status Register (A1=1,A0=1)

The status of parallel interface is a byte read out by A1=A0=1, and each bit has the following meaning.



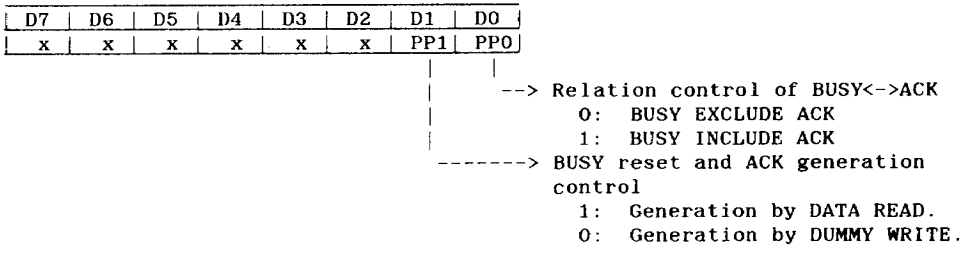
7.4 Parallel Command Register (A1=1,A0=1)

Writing (/CS=0,/WR=0,/RD=1) by A1=A0=1 serves as a command for parallel interface. (When D7=1, and D6=0.)



7.5 Parallel Mode Register (PR6)

The parameter register PR6 controls the mode of parallel interface.



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7.6 Flag and Interrupt control

The parallel input interface contains BUSY and BUFFER FULL as internal flags.

BUSY:

This flag is set at the time when external DSTB becomes active (High level). Further, this flag is set by the system reset.And also this flag is reset at the edge of ACK pulse. The direction of the edge is selected by the value of PP0. (Busy fall with ACK pulse)
Busy can be fallen without ACK generation by alternating the value of PP0. Busy_on bit in the Parallel Command Register. And the content of the Busy flag is output to the /BUSY terminal as inverce.

BUFFER FULL:

This is set at the trailing edge of external DSTB, and is reset when the CPU reads parallel data.
This is also reset by system reset.

INTERRUPT MASK:

The D5 bit of the Parallel Command Register masks the interrupt of parallel interface. When BUFFER_FULL=1 and INTM=0, a interrupt occurs from the parallel interface. The content of this occurs also in the D7 of the Parallel Status Register.

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8. USAGE OF CPC

8.1 System Interface with MPU

Fig. 8.1 shows a example of system interface.

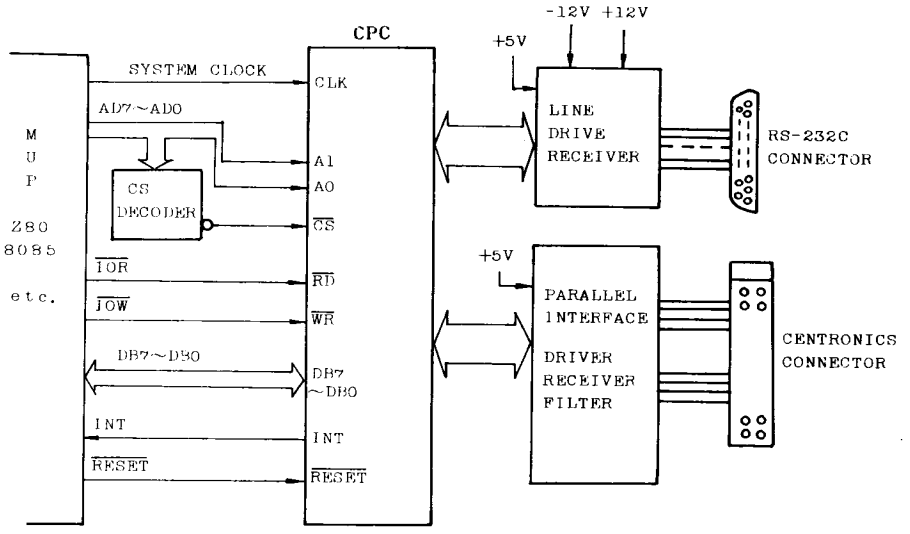

Fig. 8.1 MPU Interface

The TC8577AP or TC8576AF (CDS=0) is used for a printer driver of the like as a parallel interface.
The TC8578AP or TC8576AF (CDS=1) is used for the parallel interface receive circuits of the like in the printer.

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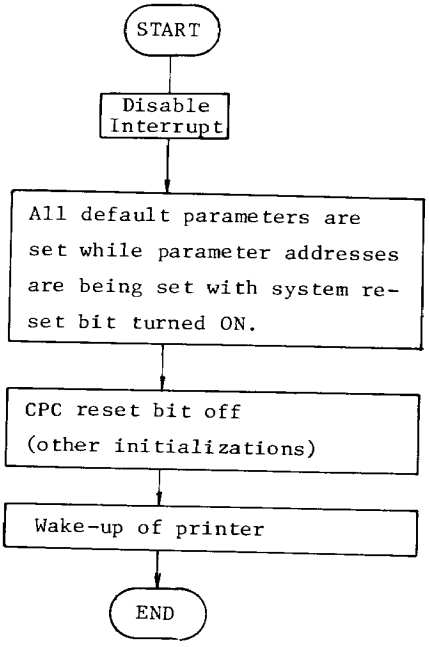
8.2 Sample of initialization program

Fig. 8.2(a) shows an example of the initialization program for driving a printer by using paraliel I/O port as output port.

This initialization program is considered as the access program to CPC the whose power is applicated.
In this case, the initialization of the parameter performed under the CPC reset condition.
For this initialization routine, the parameters are set the default value.

After completion of the initialization, the initialization for the printer is performed by giving one-shot pulse in the PRIME terminal. After that, the character string for wake-up is transferred.



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8.2 (a) Example of Initialized Program

```
;*****************************************************************
;*        CPC   INITIALIZE   PROGRAM    EXAMPLE                  *
;*                                                               *
;*     XCLK(external)        :   8MHz ( = 7,987,200 Hz)          *
;*     SYS CLK(internal)     :   2MHz ( = 1,996,800 Hz)          *
;*                                                               *
;*     CPU                   :   Z80 or equivalent               *
;*****************************************************************
     PORTCPC   EQU     0C0H              ;
     SDATA     EQU     PORTCPC+0         ; SERIAL DATA PORT (R/W)
     PDATA     EQU     PORTCPC+1         ; PARALLEL PORT    (R/W)
;
     SSTUS     EQU     PORTCPC+2         ; SERIAL STATUS    (R/O)
     PSTUS     EQU     PORTCPC+3         ; PARALLEL STATUS  (R/O)
;
     SPCON     EQU     PORTCPC+3         ; COMMAND PORT     (W/Only)
     PARAS     EQU     PORTCPC+2         ; PARAMETER SET    (W/Only)
;
     QBAUD:    DEFW    26                ; DEFAULT BAUD (9600)
                                         ;  26 = 7,987,200 / (4*9600*8)
                                         ;
               DEFB    2                 ; DEFAULT DSTB DELAY (2 usec)
               DEFB    3                 ; DEFAULT DSTB WIDTH (2 usec)
               DEFB    48                ; DEFAULT PRIME LENGTH (12.5 usec)
               DEFB    0FFH              ; DEFAULT SERIAL CHANNEL FORMAT
                                         ;   INTRRUPT NOT USE
                                         ;   EVEN-PARITY,8-BITS/CHAR,2-STOP
                                         ;
               DEFB    0                 ; DEFAULT PARALLEL MODE
               DEFB    4                 ; DEFAULT PRE-SCALER VALUE
;
INITSM:   DI                  ; DISABLE INTERRUPT
;
;    PARA METER SET
;
          LD      HL,QBAUD
          LD      A,0EOH      ; PARA-METER ADDRESS & SYSTEM RESET
          LD      B,8
          LD      C,PARAS           ; (C) IS PARAMETER PORT
INIT01:   OUT     (SPCON),A         ; SET PARAMETER ADDRESS
          INC     A                 ; SET IN NEXT ADDRESS POINTER
          OUTI                      ; SET PARAMETER FROM (HL)
          JR      NZ,INIT01
;
          LD      A,0C0H            ; RELEASE
          OUT     (SPCON),A         ; PUT IT PARAREG
;
       PRINTER WAKE UP SEQUENCE
;
```


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```
          LD      A,080H+30H+5      ; PR COMMAND 5 (PRIME ONESHOT)
                                    ;  INTERRUPT MASK
;
          OUT     (SPCON),A         ; PUT OT TO PORT
INIT11:   IN      A,(PSTUS)         ; CHECK PRIME SIGNAL
          AND     10H               ;  CHECH THE BIT
;         JR      NZ,INIT11
;  /* SOME WAIT OUTINE NEEDED FOR PRINTER READY */
;
          IN      A,(PSTUS)         ; READ PRINTER STATUS.
;
;  /* CHECK PRINTER STATUS & JUDGE SOMETHING */
;
;         JR      NZ,PRTOFF         ; IF PRINTER OFFLINE
;
          LD      HL,PRWAKE
          CALL    PROUTS
          LD      PRTOFF
;
PRWAKE:   DEFB    OFFH,OFFH,OODH,OOH
;
PRTOFF:
;
    SET ANOTHER INITIALIZE SEQUENCE
;
          JP      00000H            ; JMP TO NORMAL ENTRY
;
PROUTS    LD      A,(HL)            ; GET BYTE TO BE OUT
          OR      A                 ;  CHECK IF END (NULL)
          JR      Z,PROUTE          ;   END OF DATA
          CALL    PRCHR             ;  PUT IT PRINTER
          INC     HL                ;  (HL) POINT NEXT CHAR
          JR      PROUTS
PROUTE:   RET
;
PRCHR:    PUSH    AF                ; SAVE CHARACTER TO SEND
PRCHR:    IN      A,(PSTUS)         ; SENSE PRINTER STATUS
          AND     040H              ;  CHECK ONLY BUSY
          JR      NZ,PRCHR1         ; IF NOT READY WAIT
          POP     AF                ; RESTORE CHARACTER
          OUT     (PDATA),A         ; SEND DATA
          RET
```


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8.2(b) Example of Serial Channel

```
RSINIT:
;
;  /*  UPDATA RS-232C PARAMETER  */
;  /*    UPDATE PARAMETERS  BY READING SWITCHES
;  /*   FOR SETTING RS-232C CHANNEL PARAMETER.
;  /*   QBAUD , QBAUD+1 , QBAUD+5 MUST BE REARRANGED.
;
;
;  /*  RESET SERIAL CHANNEL  */
;
        LD      A,010H          ; ERS=1,RTS=DTR=SBRK=0,RxEN=TxEN=0
        OUT     (SPCON),A       ;  SEND IT AS COMMAND
;
;  /*  BAUD RATE SET */
;
        LD      HL,(QBAUD)      ; (HL) = BAUD RATE PARAMETER
;
        LD      A,0C0H          ; POINT TO PARA-0 (BAUD LOW)
        OUT     (SPCON),A       ;  SET IT
        LD      A,L
        OUT     (PARAS),A       ;  SET IT
;
        LD      A,0C0H          ; POINT TO PARA-1 (BAUD-HIGH)
        OUT     (SPCON),A       ;  SET IT
        LD      A,L
        OUT     (PARAS),A       ;  SET IT
;
        LD      A,0C5H          ; POINT TO PARA-5 (SERIAL MODE)
        OUT     (SPCON),A
        LD      A,(QBAUD+5)     ; FETCH PARAMETER
        OUT     (PARAS),A
;
        LD      A,027H          ; ERS=SBRK=0,RTS=DTR=RxEN=TxEN=1
        OUT     (SPCON),A       ; SEND AS A SERIAL COMMAND
;
        RET
```

Fig. 8.2(b) shows an example of a program for initializing RS-232C channel or updating Baud Rate, etc. in application programs.
Note : A separate reset should be used for initializing the CPC part in operation state.
"1" should not be programmed to D5 for address setting operation.

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9. ELECTRICAL CHARACTERISTICS

9.1 Absolute Maximum rating (VCC = +5V ± 10%)

Item	Symbol	Rating	Unit
Every Terminal Voltage		-0.5 to + 7.0	V
Operating Temperature	Topr	-40 to + 85	°C
Storage Temperature	Tstg	-65 to + 125	°C

9.2 DC characteristics

(Ta=-40°C to + 85°C, Vcc=+5V + 10%)

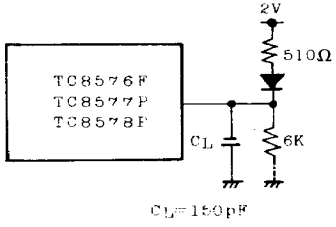
Item	Symbol	Condition	Min.	Max.	Unit
Input Low Voltage	VIL	Vcc = 5V	-0.5	0.8	V
Input High Voltage	VIH	Vcc = 5V	2.2	VCC	V
Output Low Voltage	VOL	IOL = 2.2mA	-	0.4	V
Output High Voltage	VOH	IOH = -1.1mA	4.6	-	V
Output Float Leak Current	IOFL	VOUT=0V to VCC		+10	uA
Input Leak Current	IIL	VIN = VCC to 0V		+10	uA
Supply Current	ICC			10	mA

Capacitance (Ta = 25°C, VCC = 0V)

Item	Symbol	Condition	Min.	Max.	Unit
Input Capacitance	CIN	fc = 1MHz		10	pF
I/O Capacitance	CI/O	nals used are of 0V		10	pF

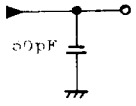
External load conditions of terminal

DB0 to DB7, INT



Bus parameter

Other output pin



I/O pin parameter

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9.3 AC characteristics

Bus parameter

Read cycle

Item	Symbol	Condition	MIN.	MAX.	UNIT
Address (A1, A0) Stability *	tAR	To formation of both	30		nS
Address (A1, A0) Hold *	tRA	of /RD and /CS	30		nS
/RD./CS Pulse width	tRR		120		nS
/RD ---> Data Delay Time	tRD	Address valid prior to /RD		120	nS
/RD ---> Data Float Delay	tDF		10	50	nS

* with relation to /RD

Write cycle

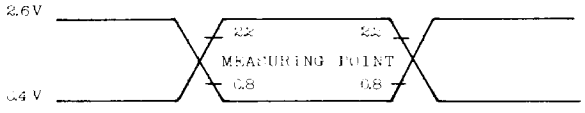
Item	Symbol	Condition	MIN.	MAX.	UNIT
Address (A1, A0) Stability *	tAW		30		nS
Address (A1, A0) Hold *	tWA		30		nS
/WR,/CS Pulse Width	tWW		120		nS
Data Set Time *	tDW		80		nS
Data Hold Time *	tWD		20		nS
Write Recovery time	tWR	(Note 1)	2		tSYS

* with relation to /RD

(Note 1)

$$tSYS = \text{internal SYS\_CLK Cycle} = \frac{1}{XCLK \times \text{Prescaler Value}}$$

AC Input Waveform for Test



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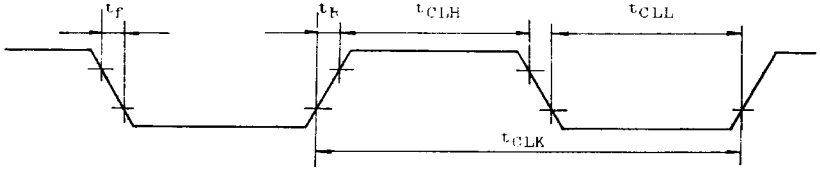
Other Timings

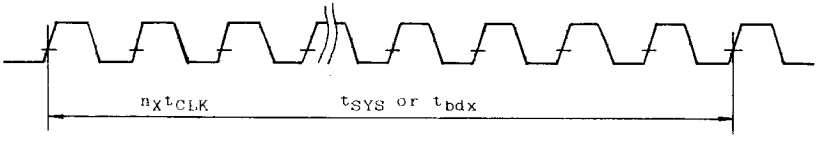
Item	Symbol	Condition	MIN.	MAX.	Unit
Clock Cycle	tCLK		0.1	3.0	uS
Clock Pulse High Level Width	tCLH		40	tCY-60	nS
Clock Pulse Low Level Width	tCLL		40	tCY-60	nS
Clock Rise or Fall Time	tR,tF		5	20	nS
Internal Clock Cycle	tSYS		160	-	nS
Baud 8x Clock Cycle	tbdx		320	-	nS
SERIAL WRITE Delay	tWS		-	140	nS
SERIAL READ Delay	tRS		-	50	nS
Parallel Data Write Delay	tWPD	CDS=0(TC8577AP)	-	140	nS
DSTB Output Delay *1	tCDSTB	CDS=0(TC8577AP)	-	130	nS
DSTB Input Pulse Width	tDSTBW	CDS=1(TC8578AP)	70	-	nS
Parallel Data Setup time *2	tDS	CDS=1(TC8578AP)	20	-	nS
Parallel Data Hold time *2	tSD	CDS=1(TC8578AP)	40	-	nS
DSTB --> /BUSY ↓	tSB	CDS=1(TC8578AP)	-	110	nS
ACK --> /BUSY ↑	tAB	CDS=1(TC8578AP)	-	110	nS
/WR --> FAULT, /PE /SLCT,/P5V	tWEX	CDS=1(TC8578AP)	-	140	nS

*1: with relation to SYS_CLK
*2: with relation to DSTB

CLK INPUT



INTERNAL CLOCK PERIOD



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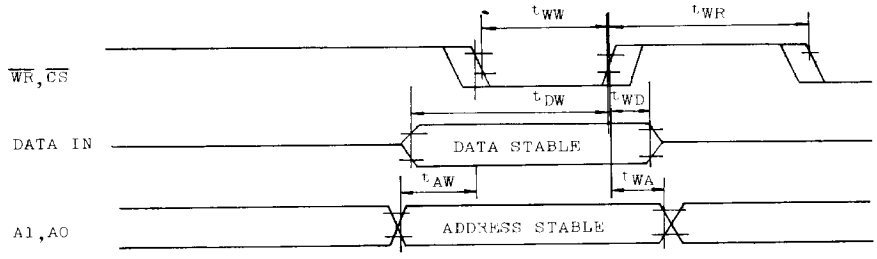
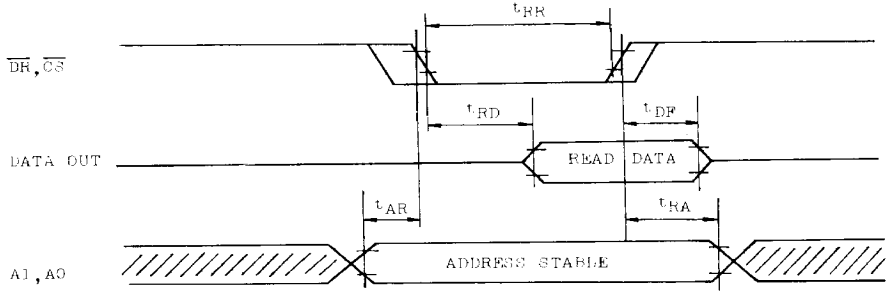
WRITE (VALID TO ALL WRITE CYCLE)

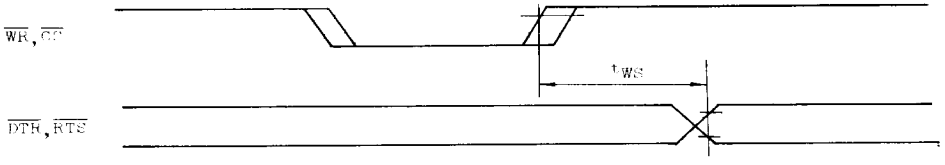


READ (VALID TO ALL READ CYCLE)

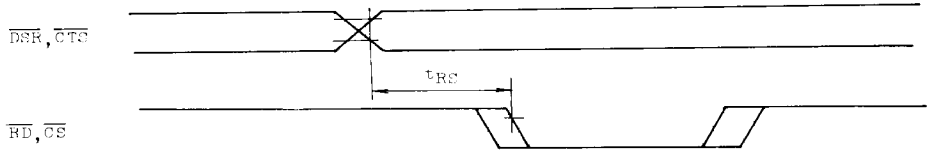


SERIAL PORT

[1] WRITE CONTROL OR OUTPUT PORT



[2] READ CONTROL OR INPUT PORT



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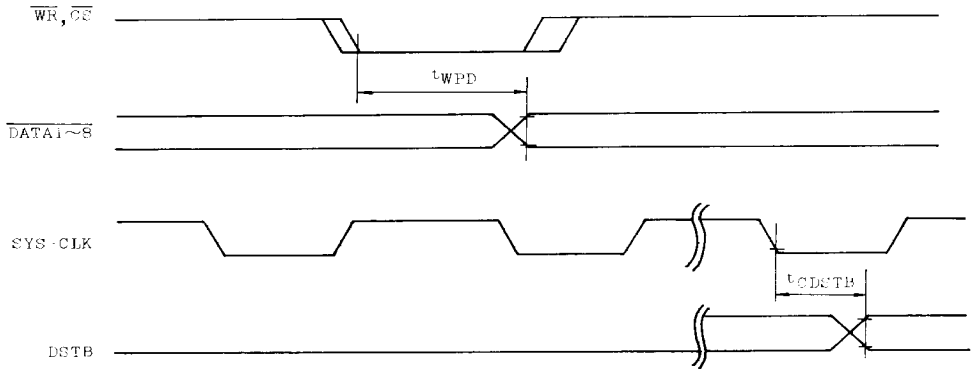
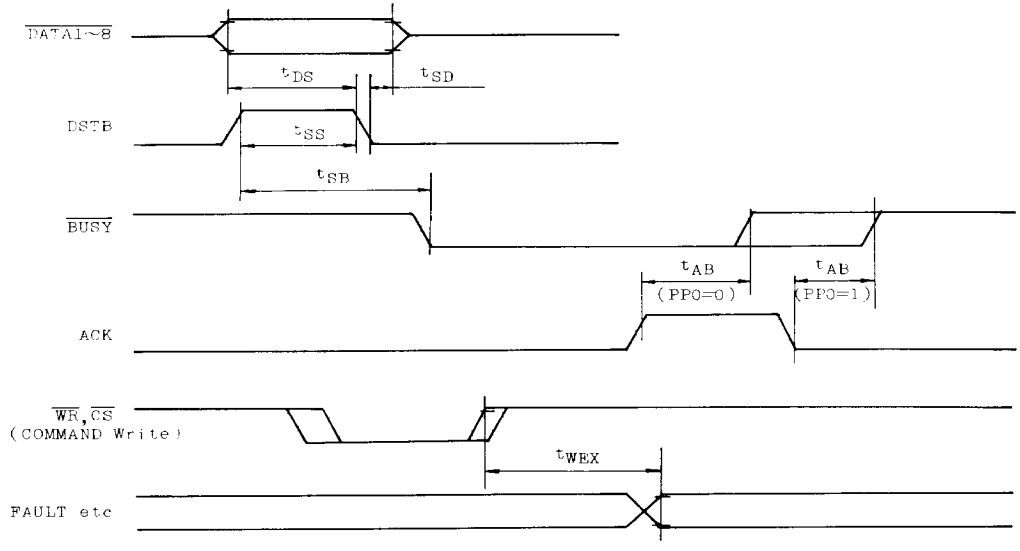
PARALLEL PORT

[1] Output Mode (CDS=0)



[2] Input Mode (CDS=1)



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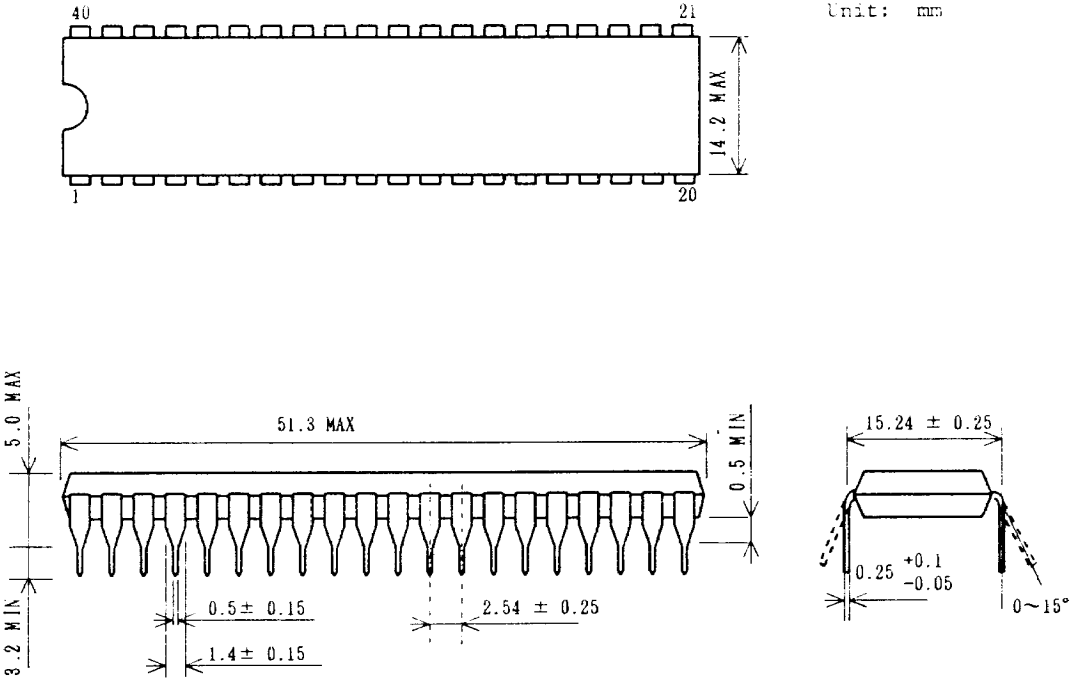
10. PACKAGE OUTLINE

40PIN DIP



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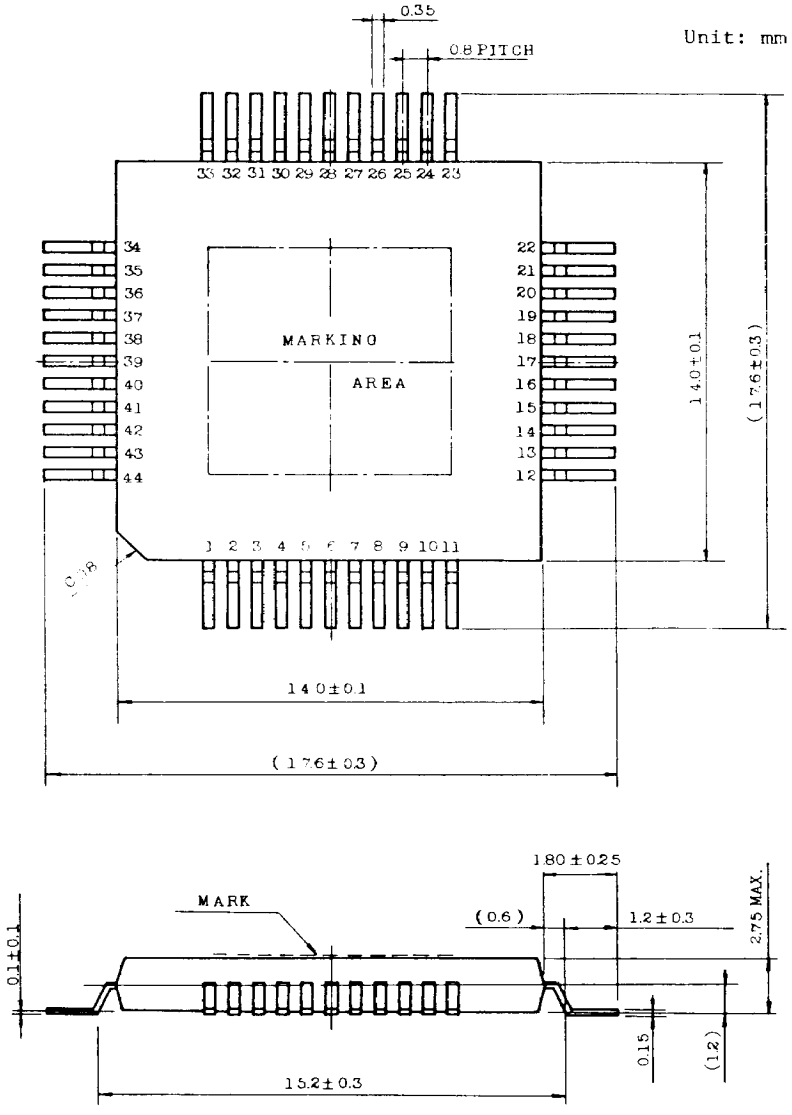
44PIN ■miniFP



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