HHC T.M.

Technical Information of the Hardware

MATSUSHITA ELECTRIC INDUSTRIAL CO., LTD.
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INTRODUCTION:

Summary of HHC Technology Breakthroughs

The HHC is far more than simply a home desk-top size computer, condensed into a hand-held portable computer. It is a totally new product concept, made possible by integratıng many truly unique state of the art technologies.

The goal was to develop a fully portable product that provided a vast range of information and communication services, that the average consumer could easily use and enjoy. To accomplish this goal required the development of sophisticated system concepts, software languages, and design techniques far beyond those found in the current generation of desk-top sized home and business computers.

FULLY VECTORED INTERRUPTS

The HHC uses 6502 MPU. Moreover, the interrupt driven I/O in the HHC makes the 6502 even significantly more powerful because it does not waste valuable processing power, normally required to monitor the keyboard, display, and peripheral devices. The result is that the HHC can execute more sophisticated applications and can handle multiple tasks at once.

BANK SELECTED MEMORY

A bank switching technique that provides extensive ROM and RAM expansion capability and flexibility.
Further, it can join ROM and RAM data via an intrinsic MEMORY CONTINUATION PROGRAM and, a new advanced MAPPING ALGORITHM design provides instant bi-directional data access for applications capsules.

"SNAP" OPERATING SYSTEM

SNAP is a new and unique software system that compacts large, complex programs into a small amount of memory space. It further enables the micro computer of the HHC to be easily and externally re-programmed via MICRO MEMORY capsule programs. As a high level programming system, SNAP is compatible with other programming languages (which can also be integrated via external memory capsules). SNAP is extremely flexible and extensible—Designed for structured programming, all system software is directly accessable by user and/or application programs without abundant overhead in execution speed and memory size.

ACHIEVING PORTABILITY AND MODULARITY

Power Saving Circuitry

In order to use the powerful, but energy consuming 6502 MPU and fast NMOS ROMs, a new powerdown circuit was developed. Thus, extended battery life is achieved and the 6502 is used in a portable computer for the first time.

Advanced Bus Architecture

Key to the modular concept, the HHC bus structure provides extended addressing, and thus virtually unlimited expansibility and interchangeability of peripheral devices. The HHC peripherals are able to work together in any combination and from any I/O slot.

MICRO MEMORY SYSTEM

The MICRO MEMORY capsules used by the HHC are the ultimate size reduction in ROM application programs. These capsules enable the HHC to achieve its small portable size and provide it with more ROM programmable power than any comparable hand-held or desk-top personal computer. Intrinsically, it holds three 16 K, 32 K, 64 K, or 128 K bit ROM capsules.

FULL MATRIX LCD GRAPHICS PANEL

A continuous dot LCD panel that facilitates graphics, foreign character alphabets, and proportional spacing, as well as full upper and lower case ASCII.

DIRECT-SIMPLIFIED-UNIFORM-KEYBOARD CONTROLS

The HHC introduces a new concept in user interface. One of the fundamental design principles is to present a simple, consistent method of entering and managing all HHC activities and key operations. Because the HHC function keys perform in a uniform fashion within all programs, it is not necessary to learn a variety of control codes, and thus the keyboard can be mastered rapidly.

SELF-INSTRUCTING MENU SYSTEM

All HHC programs (intrinsic and external) can be easily and quickly accessed via multiple-choice menus. The user reaches his activity by selecting from lists of available options presented on the display panel; or, by directly typing the proper decision key sequence, if already known.

SELF-DEFINING HHC KEYBOARD

A unique HELP key provides a definition for every HHC function key. These messages can be called up at will, even in the middle of a program or operation. The function definitions are presented on the display and thereafter the user is returned to the exact, previous, program location.

RE-ASSIGNABLE KEYBOARD

The HHC has 57 re-assignable keys, providing both a high degree of sophistication, as well as ease of operation.

SOME IMPORTANT KEYBAORD FEATURES:

—4-direction cursor/window control allows the user to ''drive'' anywhere, within any program or memory file.

—Insert and Delete keys provide flexible editting in most programs.

—Search key pinpoints desired information with a few easy keystrokes.

—A complete ASCII character set facilitates traditional command programming.

—Three user definable ''soft'' keys may be programmed with any combination of up to 15 other keystrokes, for fast input of frequently-typed sequences.

—A 10 speed display control key gives information at a user-desired rate by pressing a number from 1 (very slow) through 5 (medium) to 0 (very fast).

—Additionally, the HHC keyboard features 2-key roll over, auto-repeat keys, full cursor control, uniform exit from any program, and a keyboard overlay system—to change the total personality and/or purpose of the HHC.

THE HHC PRIMARY UNIT

The block diagram of the HHC Primary Unit is shown in Figure 1. An overview of the 6502's characteristics follows. At the end of this document is attached a full specification of the 6502.

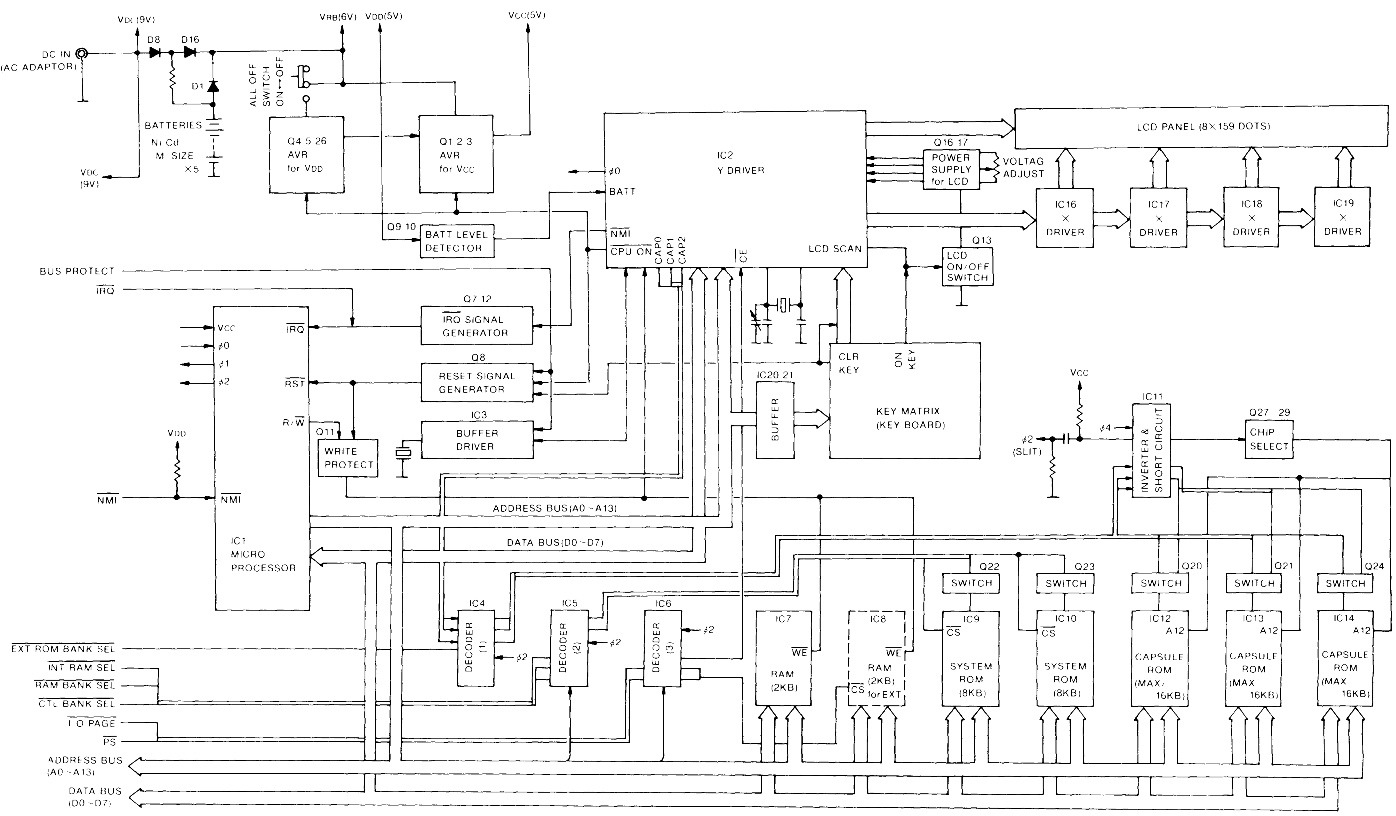


Figure 1. Block Diagram of the Primary Unit

1. CPU

Model:	RVI R6502S008 (8 Bit specified 6502 Microprocessor)
Instruction Set:	56
Addressing Modes:	13
Accumulator:	1 (A)
Index Registers:	2 (X, Y)
Other Registers:	Stack Pointer (S) Processor Status (P)
Stack:	Fixed 256 Bytes (100 to 1FF)
Status Flags:	Negative (N) Carry (C) Zero (Z) Overflow (V)
Other Flags:	IRQ Disable (I) Decimal Mode (D) BRK Command (B)
Interrupts:	2 ($\overline{IRQ}$, $\overline{NMI}$)
Reset:	1 ($\overline{RES}$)
Data Bus:	8 Bit Parallel (Bi-Directional)
Address Bus:	16 Bit Parallel
Addressable bytes in memory:	(64 KB) Locations
Supply Voltage:	5 VDC ±5%
Power Consumption:	0.25 W TYPICAL, 0.575 W MAXIMUM
Clock Frequency:	1.048576 MHz

2. LCD (LIQUID CRYSTAL DISPLAY)

8×159-dot construction plus 8 indicators; refreshed by four X driver ICs and one Y driver IC.

3. X-DRIVER

Controls 40 columns of the LCD; 160 dot columns controlled by four X driver ICs.

4. Y-DRIVER

A multiple purpose IC with several functions: Has 160 bytes of built-in dual-port RAM holding current display image. Together with X driver, provides dynamic refresh of LCD. Drives 4.194304 (MHz) crystal, producing fundamental clock operation of the system, providing timing for LCD as well as $\phi0$ clock pulse ($\phi0$ clock pulse frequency=4.194304/4=1.048576 MHz). Includes clock-driver pre-settable down counter, with 1/128 second resolution. Also accepts Keyboard-scan return signal, and, in addition to providing interrupt signal to CPU, generates Vcc power by $\overline{\text{CPU ON}}$ signal. Other functions are output by a 8-bit control register.

5. KEYBOARD

An 8×8 Key matrix designed to accept scan signal from CPU and to provide return signal to the Y driver. The CLR key controls the RESET line of the 6502, as well as being present in the keyboard matrix.

6. SYSTEM TIMING

A clock oscillator is built into the Y driver, and the $\phi0$ output from the Y driver functions as the basic timing for the CPU.

$\phi1$: phase 1 system clock (complementary with $\phi2$)
$\phi2$: phase 2 system clock (complementary with $\phi1$)

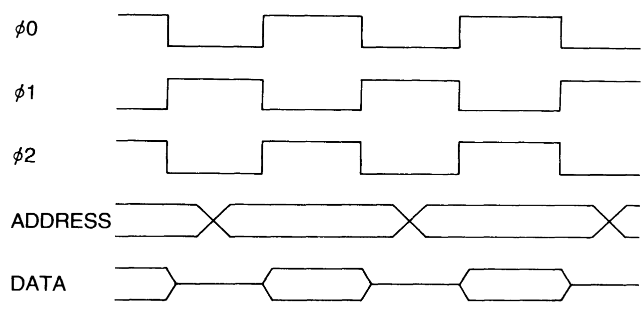


Figure 2. System Timing

7. POWER SUPPLY

VDD 5 V (Supplied to all CMOS IC's)
VCC 5 V (Supplied to all NMOS and TTL/LS circuitry, such as CPU, controlled by $\overline{\text{CPU ON}}$-signal)
VBB 5.6~7.8 V (Supplied, through a diode, from 5 built-in Ni-Cd batteries. When AC adapter used, supplied through diodes from output of AC adapter)

*Ni-Cd batteries are charged when the AC adapter is inserted (even if HHC is in use or if ALL-OFF switch is OFF).
The $\overline{\text{CPU-ON}}$ signal controlling Vcc is output from the Y driver control register. More detailed is shown in Fig. 9. (p. 14)

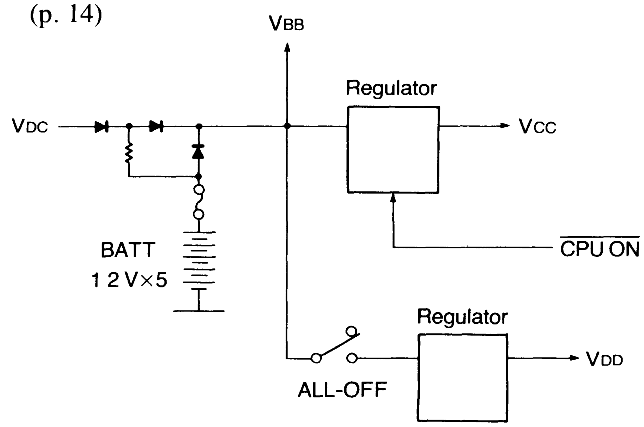


Figure 3. Power Supply

8. HHC MEMORY MAP

The memory map of the HHC is described in the table and figure 4. Two 16 K byte areas and one 8 K byte area are independently switchable banks. One 16 K byte area is used for Programmable Memory Peripherals connected to the HHC bus. Note that this area is separate from the internal RAM, which is not bank-switched. The 8 K byte area is reserved for peripheral control memory physically located in peripherals. This area can contain peripheral interrupt service routines, application programs (for example Telecomputing), and buffer RAM such as the RAM containing a video image.

The second 16 K byte area is shared between internal ROM capsules, external ROM application capsules, and I/O ports, such as keyboard and Y-driver internal to the HHC and the I/O ports in peripherals.

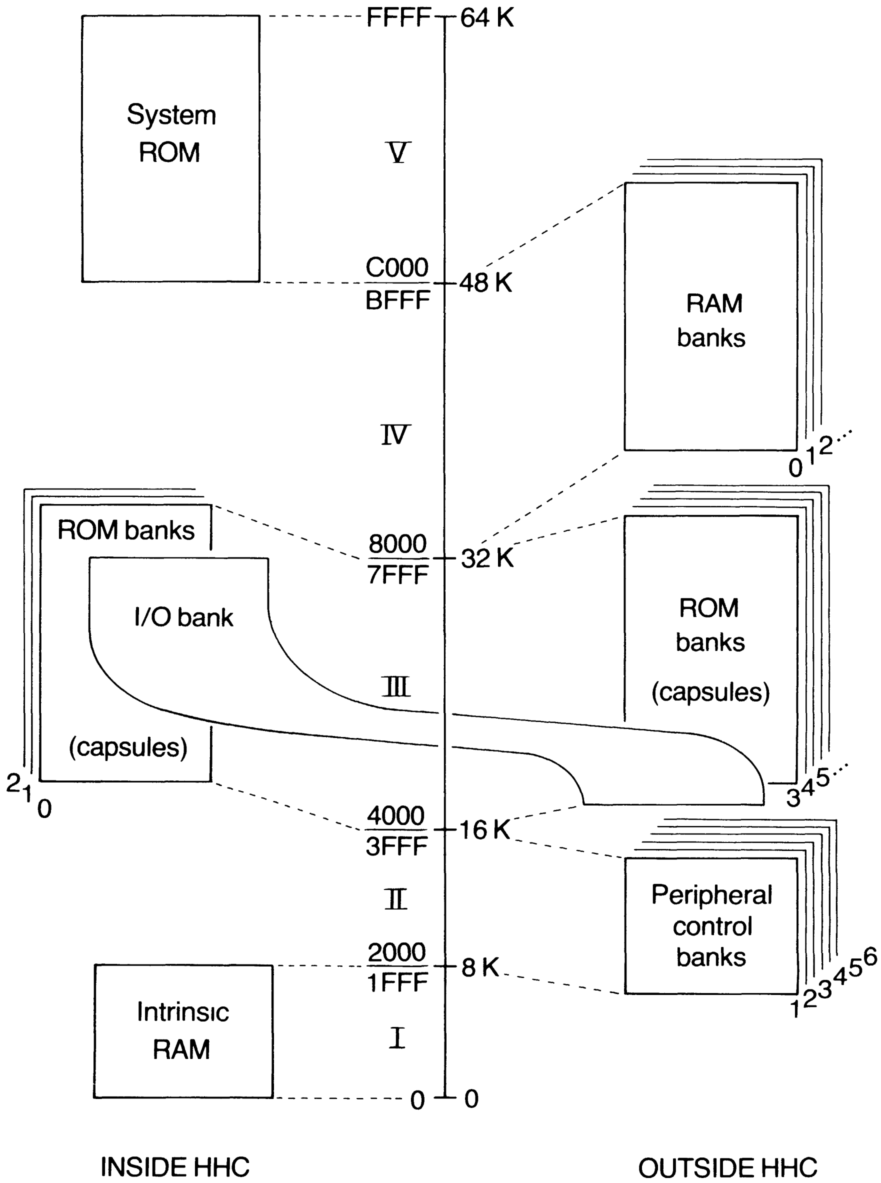


Figure 4. RAM, ROM and I/O MAP

ADDRESSES	CONTENTS	#BANKS	REMARKS
0000–1FFF	Intrinsic RAM	not switched	System variables, hardware stacks SNAP stacks, files HDTs buffers
2000–3FFF	Peripheral control	up to 16 decoded—only 6 used by I/O adaptor	Drivers start at 2000 may also contain RAM
4000–7FFF	I/O bank & ROM banks	ROMS and I/O bank	I/O always selected for write Requires select for read
8000–BFFF	RAM banks		Programmable Memory Peripherals
C000–FFFF	System ROM	not switched	SNAP nucleus, Calculator, Clock/Controller and File System

9. SYSTEM ROM

Consists of the 16 KB on the memory map from C000 to FFFF. Stores the system program and the I/O service program, as well as calculator, clock/controller, file system, and run SNAP programs.

10. EXT RAM (Peripheral—Not on Primary Unit)

Consists of 16 KB of memory from 8000 to BFFF.
The EXT. RAM is accessed when the $\overline{\text{RAM BANK SEL}}$ signal is active.

11. I/O INTERFACE AND CAPSULE

Consists of 16 KB of memory from 4000 to 7FFF. Internal Capsules are selected by capsule 1, 2 and 3 signals from Y driver.
The I/O bank from 47FC to 483B contains I/O ports dedicated to up to 16 peripherals. Each peripheral uses four consecutive locations as I/O ports. A peripheral connected directly to the HHC uses I/O ports from 47FC to 47FF. In this range, signal $\overline{\text{PS}}$ (single peripheral select) is active. Multiple peripherals are connected to the HHC through the I/O Adaptor using locations 4800 to 483B, and $\overline{\text{I/O PAGE}}$ is used. The Y-Driver and keyboard use locations 5800 to 58FF

12. CTL ROM (CONTROL ROM)

Consists of the 8 KB on the memory map from 2000 to 3FFF. Stores the peripheral control program. This space is accessed by control ROM signal and the BANK signal within the peripheral. (BANK is set only when the peripheral is accessed, and only one peripheral is selected.)

13. INT RAM (INTERNAL RAM)

Consists of the 8 KB on the memory map from 0000 to 1FFF. Up to 4 KB can be built into main unit. The INT RAM is used as the system working area and the I/O working area. The remaining areas are used for various applications, Clock/Controller messages, System files, etc.

THE INPUT/OUTPUT PORT

HHC BUS Pin Assignments & Signals

CONTROL BUS	$\overline{\text{EXT ROM BANK SEL}}$	1	2	BUS PROTECT
CONTROL BUS	V_{BB}	3	4	V_{BB}
CONTROL BUS	V_{DC}	5	6	V_{DC}
CONTROL BUS	$\overline{\text{CONTROL BANK SEL}}$	7	8	$\phi 2$
CONTROL BUS	$\overline{\text{I/O PAGE}}$	9	10	$\overline{\text{IRQ}}$
CONTROL BUS	$\overline{\text{PS}}$	11	12	BUS PROTECT
CONTROL BUS	$\overline{\text{NMI}}$	13	14	SYNC
CONTROL BUS	$R/\overline{W}$	15	16	A0
ADDRESS BUS	A1	17	18	A2
ADDRESS BUS	A3	19	20	A4
ADDRESS BUS	A5	21	22	V_{DD}
ADDRESS BUS	A6	23	24	A7
ADDRESS BUS	A8	25	26	A9
ADDRESS BUS	A10	27	28	A11
ADDRESS BUS	A12	29	30	A13
ADDRESS BUS	$\overline{\text{RAM BANK SEL}}$	31	32	$\overline{\text{INT RAM SEL}}$
DATA BUS	D0	33	34	D1
DATA BUS	D2	35	36	D3
DATA BUS	D4	37	38	D5
DATA BUS	D6	39	40	D7
	GND	41	42	GND
	V_{CC}	43	44	BUS PROTECT

NOTE: A14, A15, are not present on the bus
Even numbered pins are on the keyboard side of the HHC
Odd numbered pins are on the capsule side of the HHC

Figure 5. HHC BUS PIN ASSIGNMENTS

PIN 1. $\overline{\text{EXT ROM BANK SEL}}$
An HHC output signal which is active within the range of 4000 to 7FFF, when neither an internal capsule nor the I/O are mapped in.

PIN 2, 12, 44. BUS PROTECT
These connector pins are designed so that when peripherals are being connected to the I/O adapter, the pins make contact before any other lines, in order to protect internal operation; CPU is RESET, and when the connection is secure, the RESET is released.

PIN 3, 4. VBB
A voltage which is continuously supplied from the main unit battery. (5.6~7.8 V)

PIN 5, 6. VDC
A voltage which is supplied from AC adapter. (9 V)

PIN 7. $\overline{\text{CTL BANK SEL}}$
An active low signal used in order to access the control ROM to control each peripheral.

PIN 8. $\phi 2$
The phase 2 system clock derived from CPU.

PIN 9. $\overline{\text{I/O PAGE}}$
This active low signal decodes 4800 to 483B, used only with the I/O adapter.

PIN 10. $\overline{\text{IRQ}}$
An interrupt-request signal. When this line becomes low and the CPU accepts the interrupt, the interrupt-processing routine is executed.

PIN 11. $\overline{\text{PS}}$
The active low single peripheral select signal used by a single peripheral connected directly with the I/O Adaptor. It represents I/O slot 0, in the range of 47FC to 47FF.

PIN 13. $\overline{\text{NMI}}$
The non-maskable interrupt signal. During its transition from high to low it is recognized by the CPU. An edge-sensitive signal.

PIN 14. SYNC
An output signal which is active during the op-code fetch cycle of the CPU.

PIN 15. $\text{R}/\overline{\text{W}}$
The read/write signal. High when the CPU reads, low when it writes. Formed during $\phi 1$, self-sustaining during $\phi 2$.

PIN 16 to 30. ADDRESS (except pin 22) A0 to A13
Address bus signals formed during $\phi 1$, and is self-sustaining during $\phi 2$.

PIN 22. VDD
A +5 VDD regulated supply for the CMOS ICs. Supplied only when ALL-OFF switch is ON.

PIN 31. $\overline{\text{RAM BANK SEL}}$
A RAM BANK SELECT signal which is active in the range 8000 to BFFF.

PIN 32. $\overline{\text{INT RAM SEL}}$
A signal which is active when the CPU accesses 0000 to 1FFF.

PIN 33 to 40. DATA D0 to D7
Data-bus signals. Data is transfered during $\phi 2$.

PIN 41, 42. GND
The system ground.

PIN 43. VCC
A switched +5 VDC voltage controlled by $\overline{\text{CPU ON}}$ signal from the Y-Driver, active when the 6502 is powered.

BUS DRIVING CAPABILITY (Fan-Out)

$\overline{PS}$ .... 74LS155 decoder output
$\overline{I/O\ PAGE}$ .... 74LS155 decoder output
$\overline{BANK\ SEL}$ SIGNALS .... 74LS139 decoder outputs
$\phi 2$, R/$\overline{W}$, ADDRESS BUS, DATA BUS ..... 1 LSTTL plus 1 CMOS

NOTE: Series resistor of 1k ohm is necessary within a peripheral when driving CMOS inputs in order to protect CMOS IC's in peripherals against discharging static electricity.

BUS POWER LINES LOAD CAPABILITY

V_{DC} .... AC adapter power supply 9 V–1.2A
V_{BB} .... Battery power supply 5.6 V~7.8 V-several 100 mA
V_{CC} .... Power supply when CPU ON 5 V-about 1 mA
V_{DD} .... Power supply for CMOS gate 5 V-about 1 mA

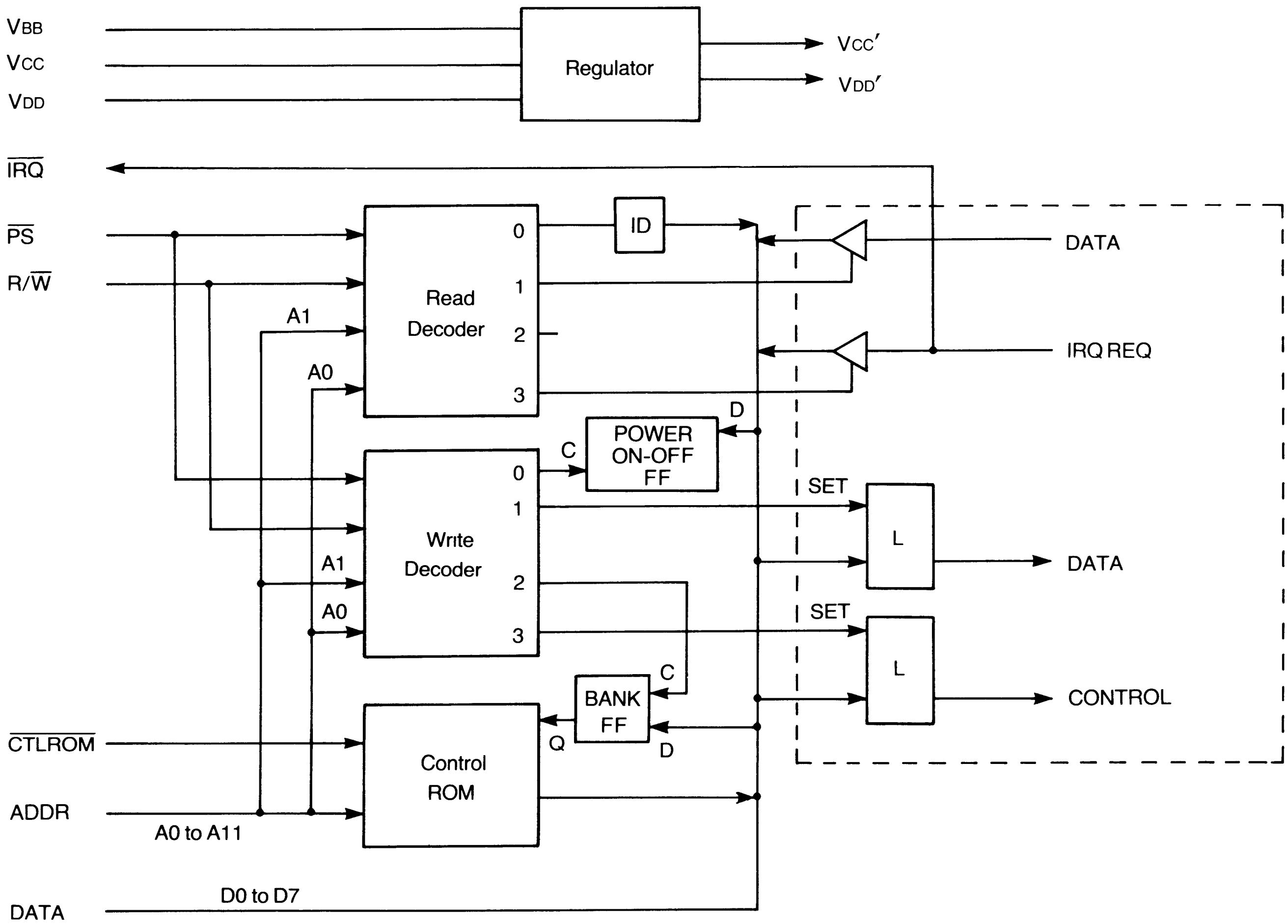


Figure 6. Block Diagram of an HHC Peripheral

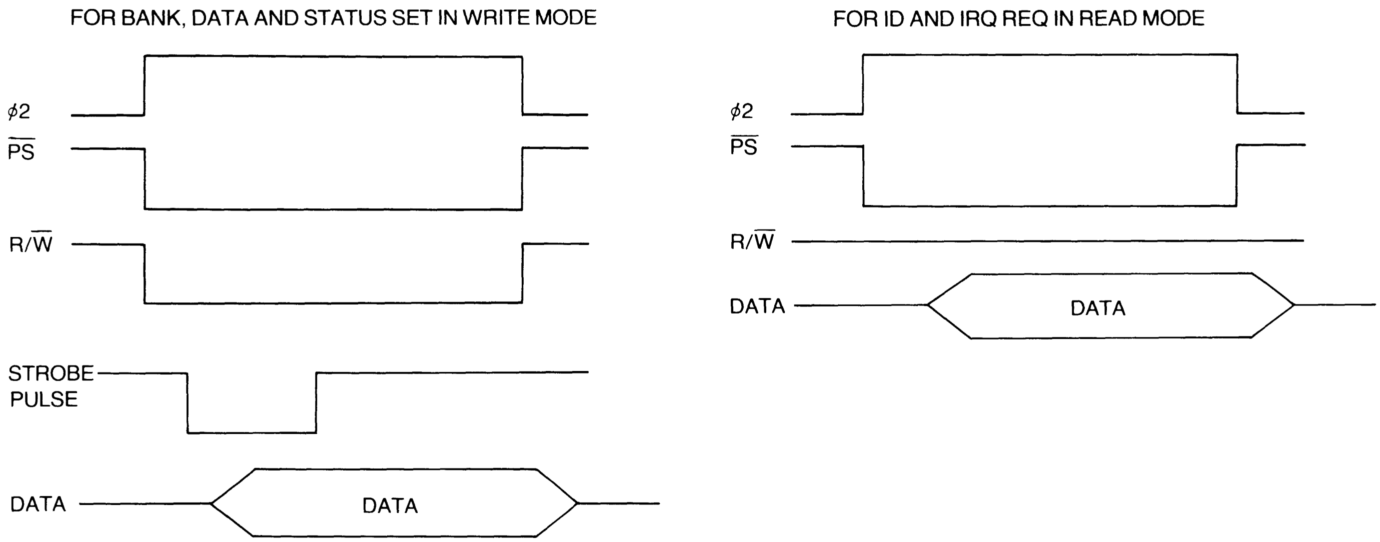


Figure 7. Peripheral Timing

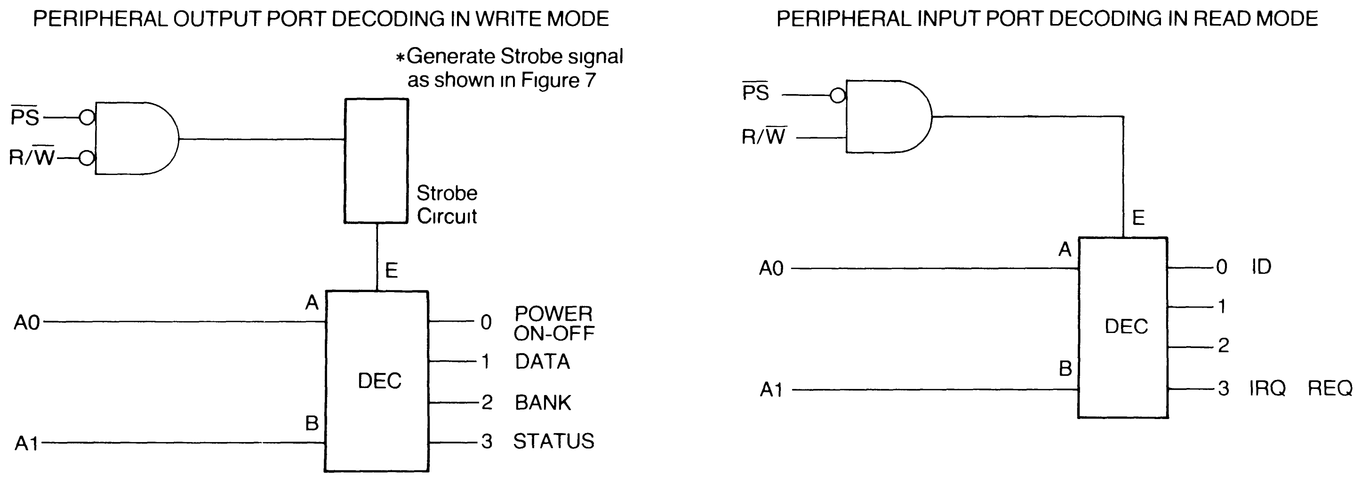
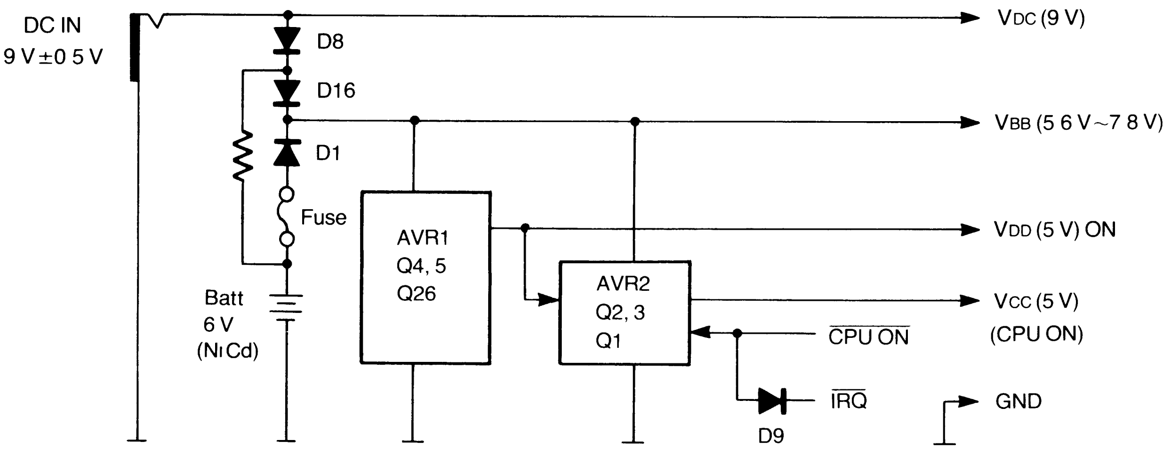


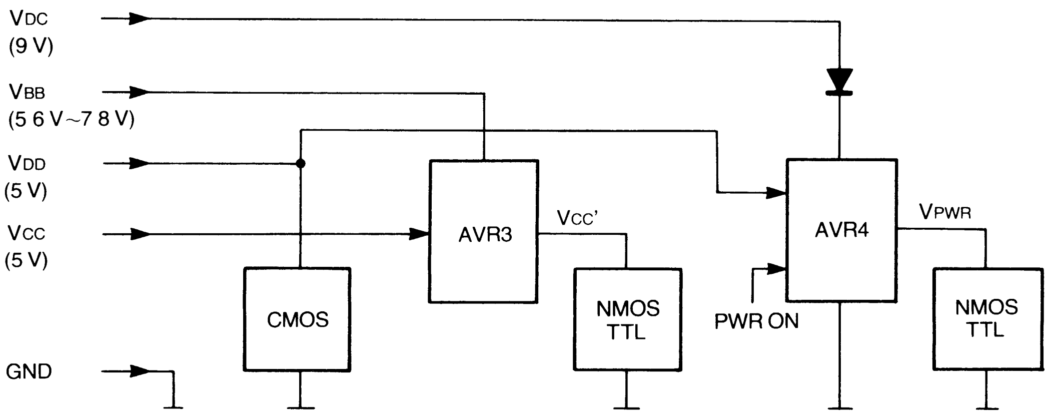
Figure 8. Peripheral Port Decoding

Primary Unit



V_{DD}	Supplied to CMOS IC
V_{CC}	Supplied to CPU Operation circuits by CPU ON signal
V_{BB}	Supplied from NiCd Battery through Diode D1 or from V_{DC} through Diode D8 & D16
V_{DC}	Supplied by AC Adaptor

Peripherals



Module Frame	V_{DC}	AVR1	AVR2	AVR3	AVR4
Primary Unit	0	0	0		
I/O RAM, ROM PRT				0	
VRAM	0			0	0
RS232C, MODEM				0	0

Note CPU ON signal that control V_{CC} is output from Y-Driver

Figure 9. Power Supply System

FUNCTION PRINCIPLE

Y-DRIVER

The Y-Driver contains a control register at 58FE that controls many important functions:
The function of the register's bits is given below

1. Control Register

Writing procedure

Input data to be written to A, X or Y. (A=accumulator, X=X resistor and Y=Y resistor)

↓

Write the data to address 58FE.

Data to be written—Control Register Configuration

D7	D6	D5	D4	D3	D2	D1	D0
M	C	B	S	L	2	1	0

M . . (Mask)

1 The address and data lines of LCD display RAM in the Y-driver are connected to CPU "1" is set for data writing-in and reading-out of the LCD display RAM. LCD display goes off.

0 . The address and data lines of LCD display RAM in the Y-driver are connected to the LCD display circuit. "0" is set for display data in the LCD display RAM. Reading and writing cannot be made through the CPU.

C . . . (CPU ON)

1 . . . $\overline{\text{CPU ON}}$ goes to L, Vcc supply circuit is turned on, and CPU operates.

0 . . . $\overline{\text{CPU ON}}$ goes to H, and CPU stops operation

B . . . (Beeper)

1 . . . Beeper output goes to H.

0 . . . Beeper output goes to L.

*Beeper sounds by inverting beeper output at the set frequency.

*Set beeper output to L before setting $\overline{\text{CPU ON}}$ to H to stop CPU operation. By doing this, the beeper will sound a warning indicating incomplete connection when a peripheral unit is connected to and disconnected from the edge connector.

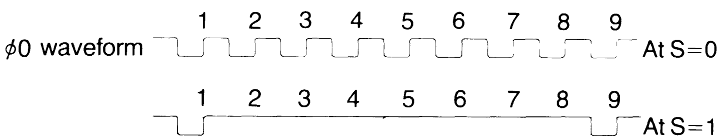
(If beeper output remains high, the beeper driving self-oscillator is damped and cannot function.)

S . . . (Slow bit)

1 . . . Slow memory cycle

0 . . . Short memory cycle

*The Y-driver oscillates at 4.194304 MHz and outputs $\phi 0$ signal at one-fourth of the frequency. It has a pulse stretch circuit to drive peripheral equipment and slow-speed devices (ROMs and RAMs)



As shown in the figure above, one period is made eight times longer. Only H level of $\phi 0$ is pulse-stretched

L . . (LCD and keyboard scan enable)

1 . . LCD scan and keyboard enable

0 . . . LCD scan and keyboard disable

$\overline{\text{CPU ON}}$ is set to H immediately after the CPU has performed required processing to stop Vcc supply, to save electricity and allow the system to be powered by a NiCd battery

Accordingly, the LCD display circuit is designed to be separately controlled so that the display can remain on while drawing minimum electricity

2 CAP 2
1 . . . CAP 1 } Each output can be set to H or L
0 . CAP 0

As shown in the memory map, area 4000–7FFF can be use by switching in read mode for effective use of memory area.

CAP2	CAP1	CAP0	(× indicates "don't care")
0	×	×	$\overline{\text{PS}}$, $\overline{\text{I/O PAGE}}$, and $\overline{\text{YDS}}$
1	0	0	INT Capsule 1 selected
1	0	1	INT Capsule 2 selected
1	1	0	INT Capsule 3 selected
1	1	1	EXT ROM bank selected

2. Timer

Timer processing is done using the presettable counter in he Y-driver.

(A) Writing to and reading from presettable counter

	Address	Input pulse	Output pulse
Lower	58FB	2^8 Hz (3 9 msec)	2^{-8} Hz (1 sec)
Middle	58FC	2^0 Hz	2^{-8} Hz (4M 27S)
Higher	58FD	2^{-8} Hz	2^{-16} Hz(18H 12M 16S)

*The lower, middle and higher presettable counters are connected in series. When the most significant digit of the higher presettable counter goes to H, keyboard sensing FF is set, $\overline{\text{CPU ON}}$ goes to L and IRQ signal is outputted Thus, CPU is turned on to perform the required processing.

*In principle, maximum resolution is 128 Hz (7.8 msec) by input clock signal of the lowest presettable counter

*In principle, CPU is turned on every time a 2^{-16} Hz signal goes to H, that is, 9H 6M 8S by the timer. In other words, current time correction is required in the minimum power consumption mode Besides the above, corrections can only be done when current time is displayed This is to save power consumption

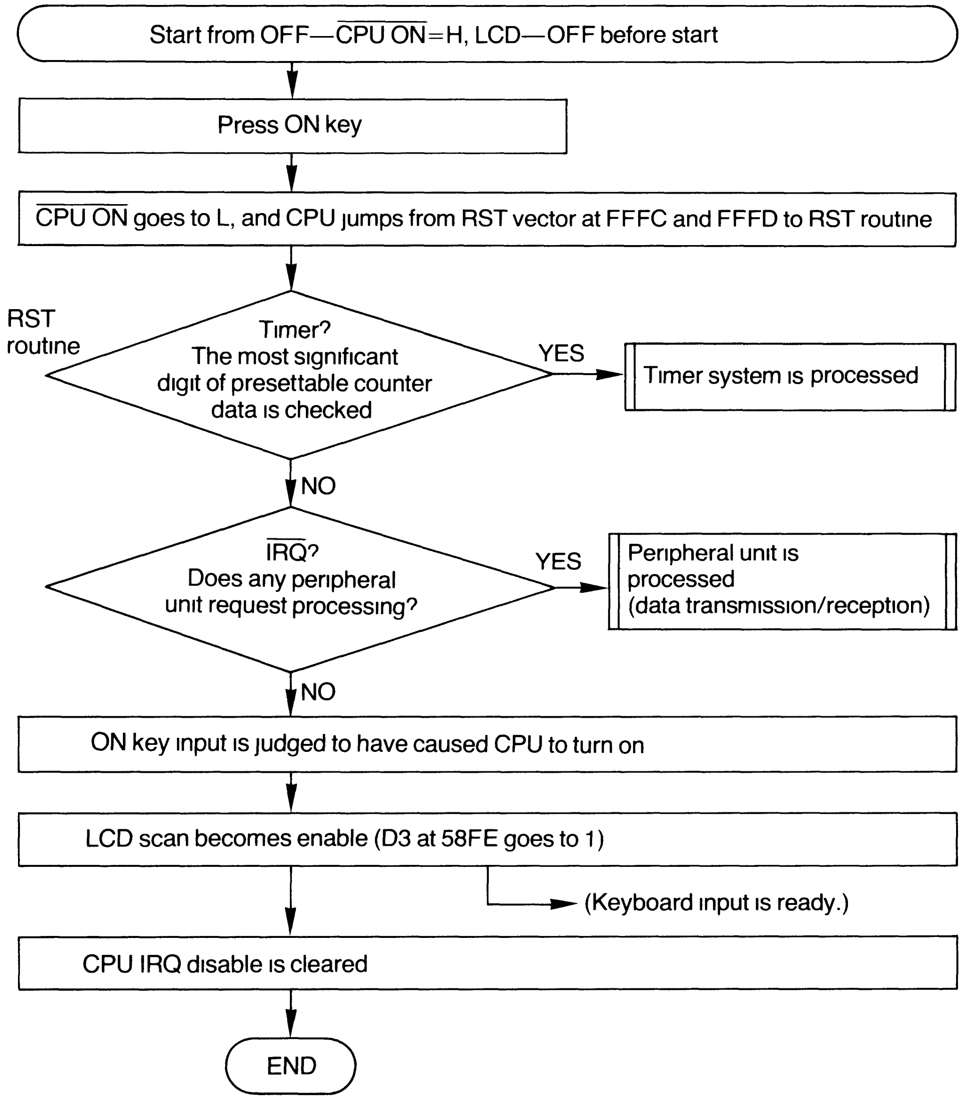
(B) Reliability of timer processing

The HHC system includes a bus protection circuit to protect timer processing when a peripheral unit is connected or disconnected The operation manual states that the set should be turned off before connection or disconnection of a peripheral unit If connection or disconnection is done during operation, timer processing is interrupted To prevent problems, timer processing is sufficiently protected by software. Processed data is written in the stack RAM at every step of timer processing When interrupted, processing returns to the step where processing has already been completed so that continuous processing can be performed For the above, a careful check is required in practical use.

3. Keyboard input

The key board matrix has three kinds of keys.

(A) ON key (ON key is acknowledged by the following procedure.)

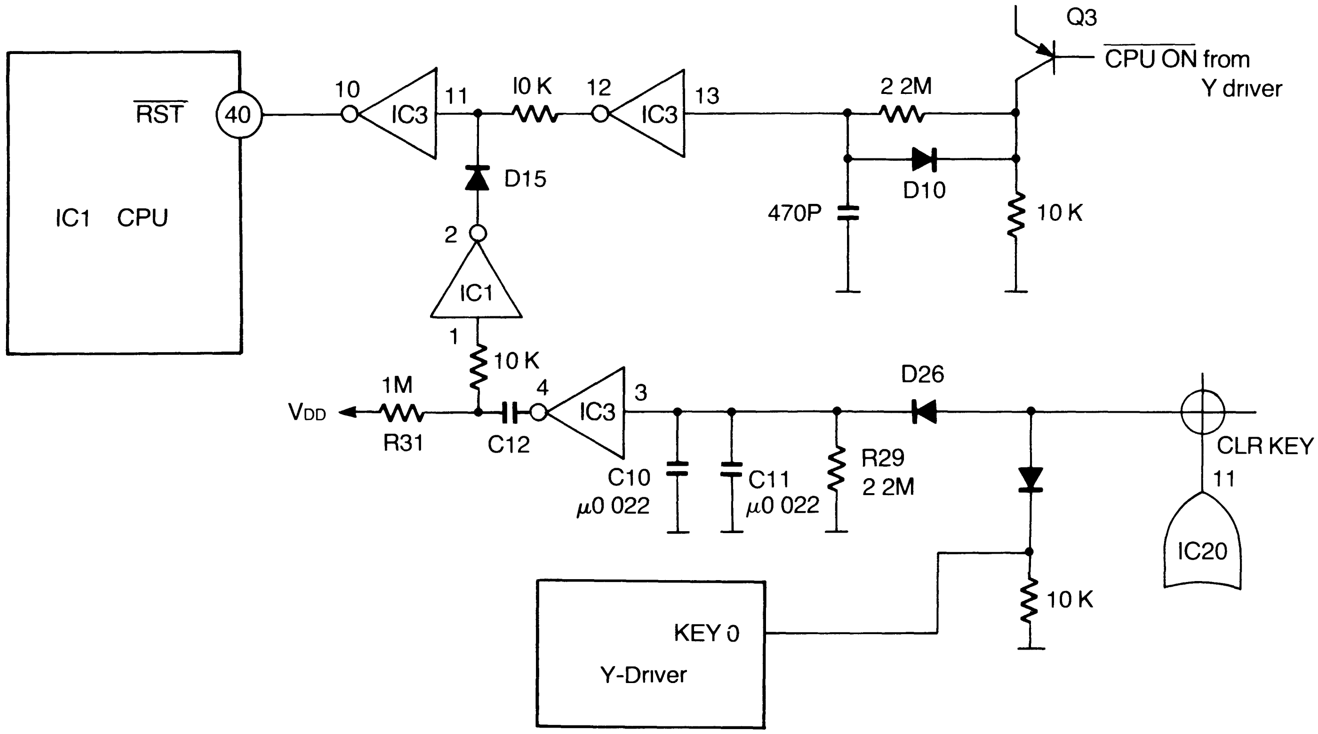


*Since causes of $\overline{\text{CPU ON}}$ cannot be checked directly, when the causes cannot be found the system judges that ON key input has been made.

*Then, CPU is turned off. If there is any processing, such as keyboard input, the system automatically clears LCD scan enable after ten minutes and turns off.

*When LCD scan is enable, no changes will occur even if ON key is pressed (for both software and hardware).

(B) CLR key



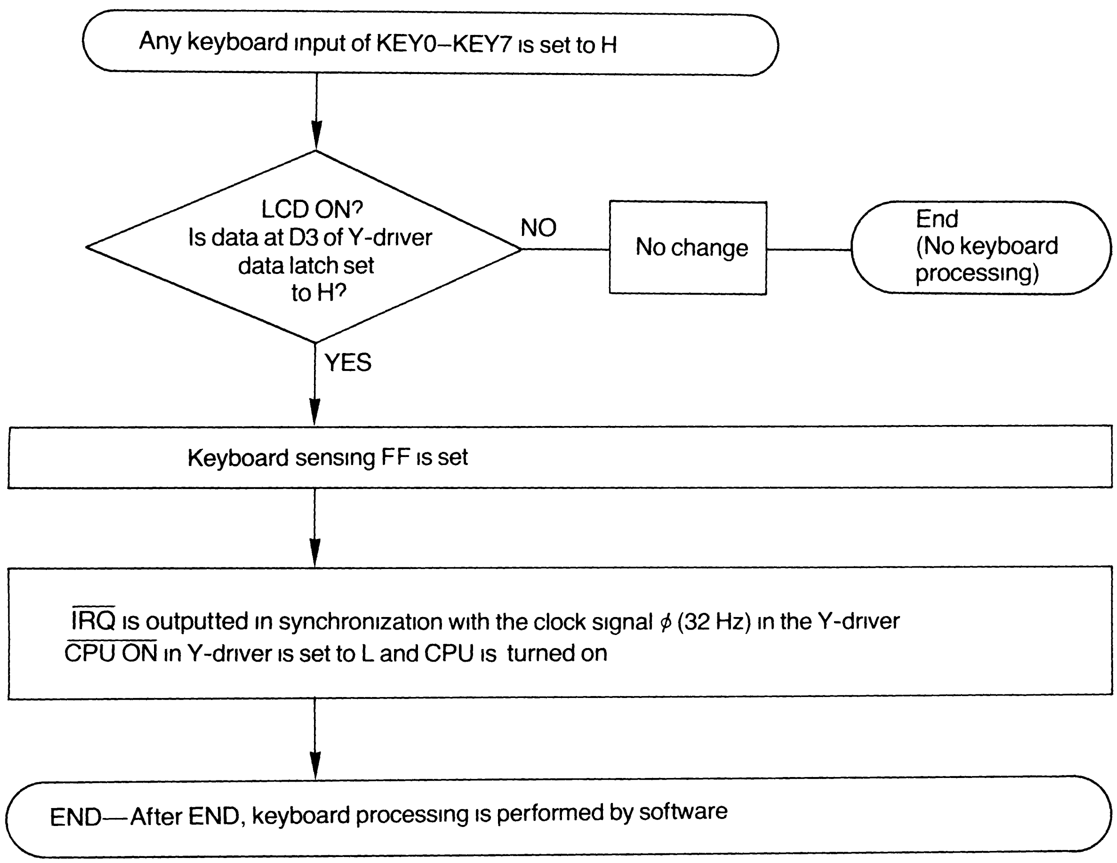
(1) Pressing the CLR key sets RST of CPU to L in the hardware. Even if CPU runs away, the system will restart from RST routine when the CLR key is pressed

(2) CLR key processing can also be done in the software. Even when the CLR key is kept pressed, RST of CPU is set to H after $\tau = 10$ msec by the differentiation circuit, composed of R31 and C12, and normal function is performed. Accordingly, since CLR key pressing can be checked by keyboard scanning, the CLR key can be used in the same way as other keys.

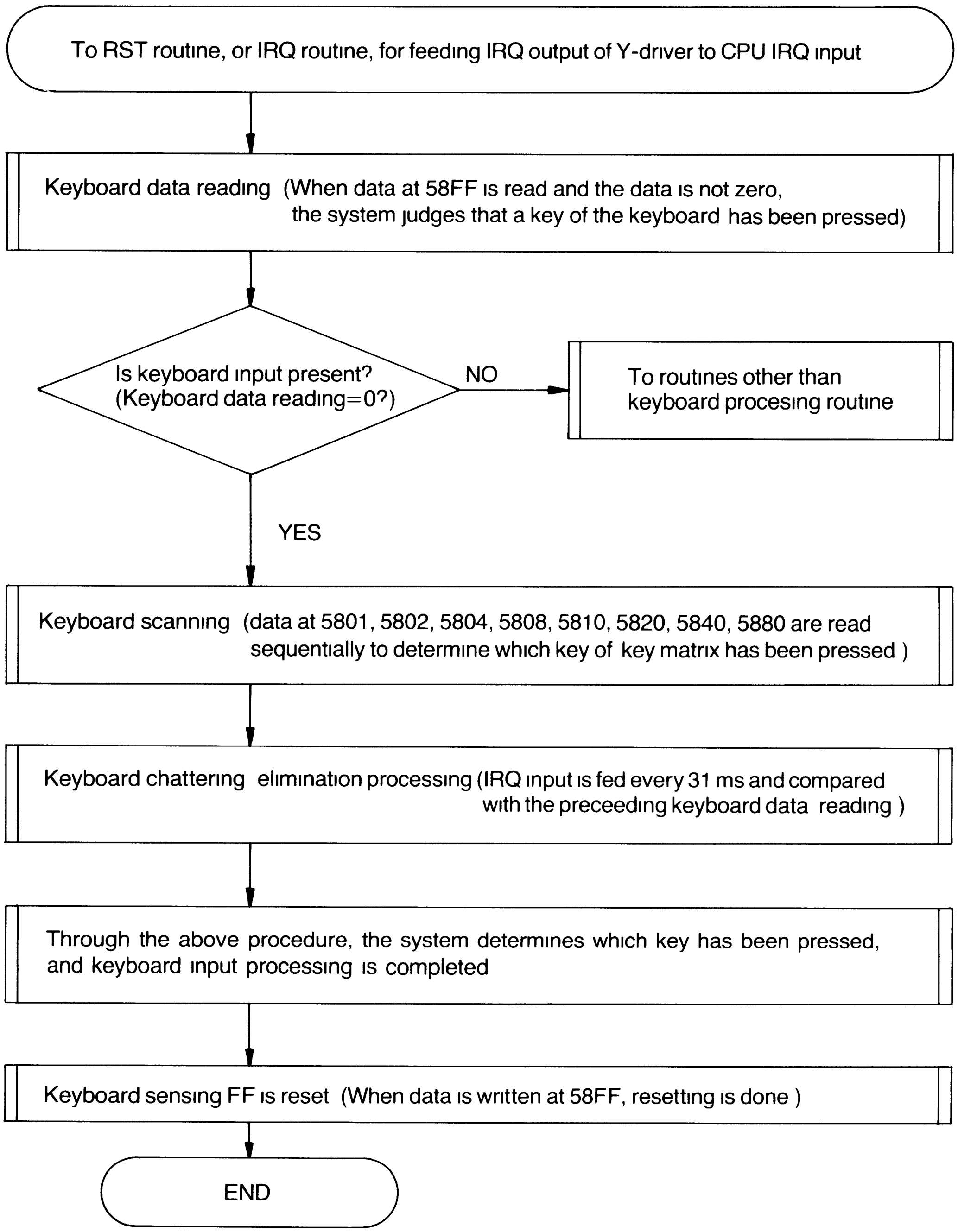
(3) If RST of CPU is set from L to H, and then set to L again within a short time, CPU will malfunction. This condition may occur when the CLR key is pressed quickly several times in succession. To prevent this, a discharging time constant of approx 100 msec ((C10 +C11) ×R29) is given after pressing the CLR key. The signal passes through the Schmitt-type CMOS inverter and is differentiated and further applied to RST of CPU.

(C) Other keys

(1) Keyboard input acceptance hard logic in Y-driver is as shown below.

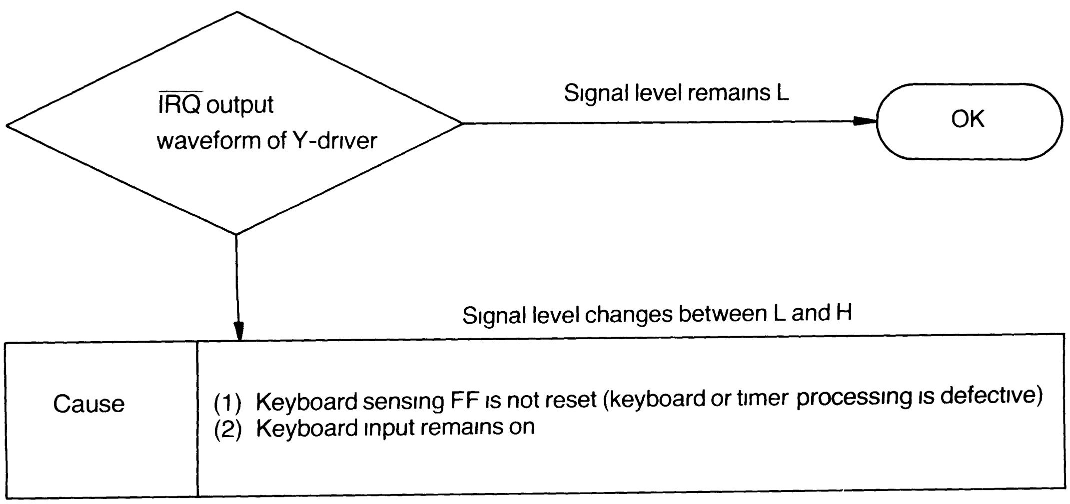


(2) Keyboard processing software routine is as shown below.



(3) Notes

*Keyboard input cannot be accepted in OFF mode, that is, while LCD scanning (display) is not being performed.
*In this OFF mode, only ON key is effective.
*In ON mode, that is, while LCD scan is enable and LCD display is functioning, keyboard input is accepted and sensing FF in Y-driver is reset to finish processing.
*Check $\overline{IRQ}$ signal waveform of Y-driver for trouble-shooting.



*In ON mode, no further changes occur when ON key is pressed again
*In ON mode, the CLR key resets RST of CPU in hardware. Then, the system software judges that the CLR key has been pressed.

R6502S008 is identical with Rockwell's standard
R6502P with the following exceptions.
Operating Temperature: −10℃ ~ +70℃
Clock Frequency: 1.2 MHz (Max.)
Read/Write Set up Time from R6500 (T_{RWS})
140 ns (Max.)
Address Set up Time from R6500 (T_{ADS})
140 ns (Max.)
Data Stability Time Period (T_{DSU})
50 ns (Min.)